Sundstrand Data Control | SUNDSTRAND AEROSPACE

REDMOND, WASHINGTON 98073 Sundstrand Corporation

WARNING COMPUTER SYSTEM

PART NUMBER

960-0284

INCLUDING

WARNING COMPUTER

965-0876-001
965-0876-030

DATA MODULE

964-0407

PROGRAM MODULE

964-0406

COMPONENT MAINTENANCE MANUAL WITH ILLUSTRATED PARTS LIST

DOCUMENT NO. 012-0598-001

NOTICE

- ***ALTERATIONS TO OR SUBSTITUTION OF PROGRAMMABLE CIRCUIT DEVICES OR ASSOCIATED CIRCUIT COMPONENTS AFFECTING DATA IN THOSE DEVICES COULD RESULT IN UNIT MALFUNCTION, ERRONEOUS OR MISLEADING DATA, OR OTHER ADVERSE EFFECTS.***
- ***IF ALTERATIONS TO PROGRAMMABLE CIRCUIT DEVICES OR ASSOCIATED CIRCUIT COMPONENTS AFFECTING THOSE DEVICES ARE NECESSARY, OBTAIN PRIOR WRITTEN SUNDSTRAND AUTHORIZATION AND INSTRUCTION BEFORE PERFORMING SUCH ALTERATION.***
- ***SUNDSTRAND ASSUMES NO LIABILITY WHATSOEVER, WHETHER CONTRACTUAL, WARRANTY, TORT OR OTHERWISE, FOR UNAUTHORIZED ALTERATION OR ALTERATIONS NOT PERFORMED IN ACCORDANCE WITH SUNDSTRAND APPROVED PROCEDURES.***

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

RECORD OF REVISIONS

REV. NO.	INSERTION DATE	BY	REV. NO.	INSERTION DATE	BY	REV. NO.	INSERTION DATE	BY
1	DEC 01/92	SDC						
2	NOV 01/93	SDC						

Retain this record in the front of manual or chapter. On receipt of revisions, insert revised pages in the manual, and enter revision number, date inserted, and initials.

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

RECORD OF TEMPORARY REVISIONS

TEMPORARY REV. NO.	ISSUE DATE	INSERTION DATE / BY	INCORPORATION DATE
34-01	APR 19/91	- - -	DEC 1/92

INCORPORATION DATE is the date of the CMM revision in which Temporary Revision information was incorporated.

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

SERVICE BULLETIN LIST

SERVICE BULLETIN NUMBER	DATE INCORPORATED	DESCRIPTION
965-0876-001-34-1 (012-0598-101)	Dec 1/92	Installs version 2.01 software which adds new aircraft types, expands the barometric altitude rate input selection, improves guidance validity logic, enhances pop-up guidance performance, and modifies the air/ground logic. It also adds a checksum for configurable parameters and miscellaneous product improvements.
965-0876-001-34-2 (012-0598-102)	Dec 1/92	Alleviates the possibility of undetected failures at high humidity and a potential timing problem which would cause the warning computer to go to the INOP state. (Mod 1)
965-0876-001-34-3 (012-0598-103)	Dec 1/92	Installs version 2.01 software which adds new aircraft types, expands the barometric altitude rate input selection, improves guidance validity logic, enhances pop-up guidance performance, and modifies the air/ground logic. It also adds a checksum for configurable parameters and miscellaneous product improvements.
965-0876-001-34-4 (012-0598-104)	Dec 1/92	Installs version 2.02 software to enhance selftest, add support for linear radio altitude, correct lamp flashing rate, add GPWC flashing lamp, change 429 output word 271 bits to match aural and visual annunciations of the warning computer, and add reasonableness test to airspeed (to detect missing or defective CIC transducers).

DATE INCORPORATED is the date of the CMM revision in which Service Bulletin information was incorporated.

SERVICE BULLETIN NUMBER	DATE INCORPORATED	DESCRIPTION
965-D876-001-34-5 (012-0598-105)	Dec 1/92	Incorporates operational and reliability improvements by correcting a microprocessor bus contention, ARINC 429 input and CMOS timing problems, and the guidance select on power-up. The service bulletin also adds isolation diodes to four discrete inputs and a fusible resistor to the power supply, changes the AC Baro Rate broken wire detection circuitry, and improves the stability of the audio circuit and dual port RAM. (Mod 2)
965-0876-0XX-34-6 (012-0598-106)	Dec 1/92	Improves the response time and accuracy of data acquisition, allowing the internal A/D converter BIT to meet the required accuracy. Failure of the A/D converter BIT will cause a WC FAIL to be logged into the warning computer's flight history. (Mod 3 for warning computer 965-0876-001-XXX-XXX) (Mod 1 for computer 965-0876-030-XXX-XXX)
965-0876-0XX-34-7	Dec 1/92	Installs version 2.03 software (B03) which adds increased warning computer functionality and corrects problems with previous releases.
965-0876-0XX-34-8 (012-0598-108)	Nov 1/93	Installs Data Module version 20.05 (B05) software which is recommended to replace existing Data Modules where the MK VII is used as a direct MK II replacement and when DC or synchro MACH is the source of airspeed. Installs Program Module version 2.04 (B04) software which adds functionality and corrects problems. Required to have new Mode 6 Menus 14, 17 and 29.

DATE INCORPORATED is the date of the CMM revision in which Service Bulletin information was incorporated.

SERVICE BULLETIN NUMBER	DATE INCORPORATED	DESCRIPTION
965-0876-0XX-34-9 (012-0598-109)	Nov 1/93	Adds discrete validities to computed pitch and roll rates. Highly recommended for guidance customers. See Service Bulletin for additional reasons.
965-0876-001-34-10 (012-0598-110)	Nov 1/93	Mod to improve operation and reliability. Mod 4. Mfg on SN 2080 and on.
965-0876-030-34-11 (012-0598-111)	Nov 1/93	Mod to improve operation and reliability. Mod 2. Mfg on SN 2080 and on.

DATE INCORPORATED is the date of the CMM revision in which Service Bulletin information was incorporated.

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

LIST OF EFFECTIVE PAGES

PAGE	DATE
T-1	Nov 01/93
T-2	Blank
RR-1	Nov 01/93
RR-2	Blank
TR-1	Nov 01/93
TR-2	Blank
SB-1	Nov 01/93
SB-2	Nov 01/93
SB-3	Nov 01/93
SB-4	Blank
LEP-1	Nov 01/93
LEP-2	Nov 01/93
LEP-3	Nov 01/93
LEP-4	Nov 01/93
LEP-5	Nov 01/93
LEP-6	Blank
TC-1	Nov 01/93
TC-2	Nov 01/93
TC-3	Nov 01/93
TC-4	Nov 01/93
TC-5	Nov 01/93
TC-6	Nov 01/93
TC-7	Nov 01/93
Intro-1	Nov 01/93
Intro-2	Nov 01/93
Intro-3	Nov 01/93
Intro-4	Nov 01/93
1	Nov 01/93
2	Nov 01/93
3	Nov 01/93
4	Nov 01/93
5	Nov 01/93
6	Nov 01/93
7	Nov 01/93
8	Nov 01/93
9	Nov 01/93
10	Nov 01/93
11	Nov 01/93
12	Nov 01/93
13	Nov 01/93
14	Nov 01/93
15	Nov 01/93
16	Nov 01/93
17	Nov 01/93
18	Nov 01/93
19	Nov 01/93
20	Nov 01/93
21	Nov 01/93
22	Nov 01/93
23	Nov 01/93
24	Nov 01/93
25	Nov 01/93
26	Nov 01/93
27	Nov 01/93
28	Nov 01/93
29	Nov 01/93
30	Nov 01/93
31	Nov 01/93
32	Nov 01/93
33	Nov 01/93
34	Nov 01/93
35	Nov 01/93
36	Nov 01/93
37	Nov 01/93
38	Nov 01/93
39	Nov 01/93
40	Nov 01/93
41	Nov 01/93
42	Nov 01/93
43	Nov 01/93
44	Nov 01/93
45	Nov 01/93
46	Nov 01/93
47	Nov 01/93
48	Nov 01/93
49	Nov 01/93
50	Nov 01/93
51	Nov 01/93
52	Nov 01/93
53	Nov 01/93
54	Nov 01/93
55	Nov 01/93
56	Nov 01/93
57	Nov 01/93
58	Nov 01/93
59	Nov 01/93
60	Nov 01/93
61	Nov 01/93
62	Nov 01/93
63	Nov 01/93
64	Nov 01/93
65	Nov 01/93
66	Nov 01/93
67	Nov 01/93
68	Nov 01/93
69	Nov 01/93
70	Nov 01/93
71	Nov 01/93
72	Nov 01/93
73	Nov 01/93
74	Nov 01/93
75	Nov 01/93
76	Blank
101	Nov 01/93
102	Nov 01/93
103	Nov 01/93
104	Nov 01/93
105	Nov 01/93
106	Nov 01/93
107	Nov 01/93
108	Nov 01/93
109	Nov 01/93
110	Nov 01/93
111	Nov 01/93
112	Nov 01/93
113	Nov 01/93
114	Nov 01/93
115	Nov 01/93
116	Nov 01/93
117	Nov 01/93
118	Nov 01/93
119	Nov 01/93
120	Nov 01/93
121	Nov 01/93
122	Nov 01/93
123	Nov 01/93
124	Nov 01/93
125	Nov 01/93
126	Nov 01/93
127	Nov 01/93
128	Nov 01/93
129	Nov 01/93
130	Nov 01/93
131	Nov 01/93
132	Nov 01/93
133	Nov 01/93
134	Nov 01/93
135	Nov 01/93
136	Nov 01/93

PAGE	DATE
137	Nov 01/93
138	Nov 01/93
139	Nov 01/93
140	Nov 01/93
141	Nov 01/93
142	Nov 01/93
143	Nov 01/93
144	Nov 01/93
145	Nov 01/93
146	Nov 01/93
147	Nov 01/93
148	Blank
149	Nov 01/93
150	Blank
151	Nov 01/93
152	Blank
153	Nov 01/93
154	Blank
155	Nov 01/93
156	Blank
157	Nov 01/93
158	Blank
159	Nov 01/93
160	Blank
161	Nov 01/93
162	Blank
163	Nov 01/93
164	Blank
165	Nov 01/93
166	Blank
167	Nov 01/93
168	Blank
169	Nov 01/93
170	Blank
171	Nov 01/93
172	Blank
173	Nov 01/93
174	Blank
175	Nov 01/93
176	Blank
177	Nov 01/93
178	Blank
179	Nov 01/93
180	Blank
181	Nov 01/93
182	Blank
183	Nov 01/93
184	Blank
185	Nov 01/93
186	Blank
187	Nov 01/93
188	Blank
189	Nov 01/93
190	Blank
191	Nov 01/93
192	Blank
193	Nov 01/93
194	Blank
195	Nov 01/93
196	Blank
197	Nov 01/93
198	Blank
198.1	Nov 01/93
198.2	Blank
198.3	Nov 01/93
198.4	Blank
198.5	Nov 01/93
198.6	Blank
198.7	Nov 01/93
198.8	Blank
198.9	Nov 01/93
198.10	Blank
198.11	Nov 01/93
198.12	Blank
198.13	Nov 01/93
198.14	Blank
198.15	Nov 01/93
198.16	Blank
198.17	Nov 01/93
198.18	Blank
198.19	Nov 01/93
198.20	Blank
198.21	Nov 01/93
198.22	Blank
198.23	Nov 01/93
198.24	Blank
198.25	Nov 01/93
198.26	Blank
198.27	Nov 01/93
198.28	Blank
198.29	Nov 01/93
198.30	Blank
198.31	Nov 01/93
198.32	Blank
198.33	Nov 01/93
198.34	Blank
198.35	Nov 01/93
198.36	Blank
198.37	Nov 01/93
198.38	Blank
198.39	Nov 01/93
198.40	Blank
198.41	Nov 01/93
198.42	Blank
198.43	Nov 01/93
198.44	Blank
198.45	Nov 01/93
198.46	Blank
198.47	Nov 01/93
198.48	Blank
198.49	Nov 01/93
198.50	Blank
198.51	Nov 01/93
198.52	Blank
198.53	Nov 01/93
198.54	Blank
198.55	Nov 01/93
198.56	Blank
198.57	Nov 01/93
198.58	Blank
198.59	Nov 01/93
198.60	Blank
198.61	Nov 01/93
198.62	Blank
198.63	Nov 01/93
198.64	Blank
198.65	Nov 01/93
198.66	Blank
198.67	Nov 01/93
198.68	Blank
198.69	Nov 01/93
198.70	Blank
198.71	Nov 01/93
198.72	Blank
198.73	Nov 01/93
198.74	Blank
198.75	Nov 01/93
198.76	Blank
198.77	Nov 01/93
198.78	Blank
198.79	Nov 01/93
198.80	Blank
198.81	Nov 01/93
198.82	Blank
198.83	Nov 01/93
198.84	Blank
198.85	Nov 01/93
198.86	Blank
198.87	Nov 01/93
198.88	Blank
198.89	Nov 01/93
198.90	Blank
198.91	Nov 01/93

PAGE	DATE
198.92	Blank
198.93	Nov 01/93
198.94	Blank
198.95	Nov 01/93
198.96	Blank
198.97	Nov 01/93
198.98	Blank
198.99	Nov 01/93
198.100	Blank
198.101	Nov 01/93
198.102	Blank
198.103	Nov 01/93
198.104	Blank
198.105	Nov 01/93
198.106	Blank
198.107	Nov 01/93
198.108	Blank
198.109	Nov 01/93
198.110	Blank
198.111	Nov 01/93
198.112	Blank
198.113	Nov 01/93
198.114	Blank
198.115	Nov 01/93
198.116	Blank
198.117	Nov 01/93
198.118	Blank
198.119	Nov 01/93
198.120	Blank
198.121	Nov 01/93
198.122	Blank
198.123	Nov 01/93
198.124	Blank
198.125	Nov 01/93
198.126	Blank
198.127	Nov 01/93
198.128	Blank
198.129	Nov 01/93
198.130	Blank
198.131	Nov 01/93
198.132	Blank
198.133	Nov 01/93
198.134	Blank
198.135	Nov 01/93
198.136	Blank
198.137	Nov 01/93
198.138	Blank
198.139	Nov 01/93
198.140	Blank
198.141	Nov 01/93
198.142	Blank
198.143	Nov 01/93
198.144	Blank
198.145	Nov 01/93
198.146	Blank
198.147	Nov 01/93
198.148	Blank
198.149	Nov 01/93
198.150	Blank
198.151	Nov 01/93
198.152	Blank
198.153	Nov 01/93
198.154	Blank
198.155	Nov 01/93
198.156	Blank
198.157	Nov 01/93
198.158	Blank
198.159	Nov 01/93
198.160	Blank
198.161	Nov 01/93
198.162	Blank
198.163	Nov 01/93
198.164	Blank
198.165	Nov 01/93
198.166	Blank
198.167	Nov 01/93
198.168	Blank
198.169	Nov 01/93
198.170	Blank
198.171	Nov 01/93
198.172	Blank
198.173	Nov 01/93
198.174	Blank
198.175	Nov 01/93
198.176	Blank
198.177	Nov 01/93
198.178	Blank
198.179	Nov 01/93
198.180	Blank
198.181	Nov 01/93
198.182	Blank
198.183	Nov 01/93
198.184	Blank
198.185	Nov 01/93
198.186	Blank
198.187	Nov 01/93
198.188	Blank
198.189	Nov 01/93
198.190	Blank
198.191	Nov 01/93
198.192	Blank
198.193	Nov 01/93
198.194	Blank
198.195	Nov 01/93
198.196	Blank
198.197	Nov 01/93
198.198	Blank
198.199	Nov 01/93
198.200	Blank
198.201	Nov 01/93
198.202	Blank
198.203	Nov 01/93
198.204	Blank
198.205	Nov 01/93
198.206	Blank
198.207	Nov 01/93
198.208	Blank
198.209	Nov 01/93
198.210	Blank
198.211	Nov 01/93
198.212	Blank
198.213	Nov 01/93
198.214	Blank
198.215	Nov 01/93
198.216	Blank
198.217	Nov 01/93
198.218	Blank
198.219	Nov 01/93
198.220	Blank
198.221	Nov 01/93
198.222	Blank
198.223	Nov 01/93
198.224	Blank
198.225	Nov 01/93
198.226	Blank
198.227	Nov 01/93
198.228	Blank
198.229	Nov 01/93
198.230	Blank
198.231	Nov 01/93
198.232	Blank
198.233	Nov 01/93
198.234	Blank
198.235	Nov 01/93
198.236	Blank
198.237	Nov 01/93
198.238	Blank
198.239	Nov 01/93
198.240	Blank
198.241	Nov 01/93
198.242	Blank
198.243	Nov 01/93
198.244	Nov 01/93

PAGE	DATE
198.245	Nov 01/93
198.246	Blank
198.247	Nov 01/93
198.248	Blank
198.249	Nov 01/93
198.250	Blank
198.251	Nov 01/93
198.252	Blank
198.253	Nov 01/93
198.254	Blank
198.255	Nov 01/93
198.256	Blank
198.257	Nov 01/93
198.258	Blank
198.259	Nov 01/93
198.260	Blank
198.261	Nov 01/93
198.262	Blank
198.263	Nov 01/93
198.264	Blank
198.265	Nov 01/93
198.266	Blank
198.267	Nov 01/93
198.268	Blank
198.269	Nov 01/93
198.270	Blank
198.271	Nov 01/93
198.272	Blank
198.273	Nov 01/93
198.274	Blank
198.275	Nov 01/93
198.276	Blank
198.277	Nov 01/93
198.278	Blank
198.279	Nov 01/93
198.280	Blank
198.281	Nov 01/93
198.282	Blank
198.283	Nov 01/93
198.284	Blank
198.285	Nov 01/93
198.286	Blank
198.287	Nov 01/93
198.288	Blank
198.289	Nov 01/93
198.290	Nov 01/93
198.291	Nov 01/93
198.292	Nov 01/93
198.293	Nov 01/93
198.294	Nov 01/93
198.295	Nov 01/93
198.296	Nov D1/93
198.297	Nov 01/93
198.298	Nov 01/93
198.299	Nov 01/93
198.300	Nov 01/93
198.301	Nov 01/93
198.302	Nov 01/93
198.303	Nov 01/93
198.304	Nov 01/93
198.305	Nov 01/93
198.306	Nov 01/93
198.307	Nov 01/93
198.308	Nov 01/93
198.309	Nov 01/93
198.310	Nov 01/93
198.311	Nov 01/93
198.312	Nov 01/93
301	Nov 01/93
302	Nov 01/93
303	Nov 01/93
304	Blank
401	Nov 01/93
402	Nov 01/93
403	Nov 01/93
404	Blank
501	Nov 01/93
502	Blank
601	Nov 01/93
602	Nov 01/93
701	Nov 01/93
702	Nov 01/93
703	Nov 01/93
704	Nov 01/93
705	Nov 01/93
706	Nov 01/93
707	Nov 01/93
708	Nov 01/93
709	Nov 01/93
710	Blank
801	Nov 01/93
802	Blank
901	Nov 01/93
902	Nov 01/93
1001	Nov 01/93
1002	Nov 01/93
1003	Nov 01/93
1004	Nov 01/93
1005	Nov 01/93
1006	Nov 01/93
1007	Nov 01/93
1008	Nov 01/93
1009	Nov 01/93
1010	Nov 01/93
1011	Nov 01/93
1012	Nov 01/93
1013	Nov 01/93
1014	Nov 01/93
1015	Nov 01/93
1016	Nov 01/93
1017	Nov 01/93
1018	Nov 01/93
1019	Nov 01/93
1020	Nov 01/93
1021	Nov 01/93
1022	Nov 01/93
1023	Nov 01/93
1024	Nov 01/93
1025	Nov 01/93
1026	Nov 01/93
1027	Nov 01/93
1028	Nov 01/93
1029	Nov 01/93
1030	Nov 01/93
1031	Nov 01/93
1032	Nov 01/93
1033	Nov 01/93
1034	Nov 01/93
1035	Nov 01/93
1036	Nov 01/93
1037	Nov 01/93
1038	Nov 01/93
1039	Nov 01/93
1040	Nov 01/93
1041	Nov 01/93
1042	Nov 01/93
1043	Nov 01/93
1044	Nov 01/93
1045	Blank
1046	Nov 01/93
1047	Nov 01/93
1048	Nov 01/93
1049	Nov 01/93
1050	Blank
1051	Blank

PAGE	DATE
1052	Nov 01/93
1053	Nov 01/93
1054	Nov 01/93
1055	Nov 01/93
1056	Nov 01/93
1057	Nov 01/93
1058	Blank
1059	Blank
1060	Nov 01/93
1061	Blank
1062	Nov 01/93
1063	Blank
1064	Nov 01/93
1065	Blank
1066	Nov 01/93
1067	Blank
1068	Nov 01/93
1069	Blank
1070	Nov 01/93
1071	Nov 01/93
1072	Nov 01/93
1073	Nov 01/93
1074	Nov 01/93
1075	Nov 01/93
1076	Nov 01/93
1077	Nov 01/93
1078	Nov 01/93
1079	Nov 01/93
1080	Nov 01/93
1081	Nov 01/93
1082	Nov 01/93
1083	Nov 01/93
1084	Nov 01/93
1085	Nov 01/93
1086	Nov 01/93
1087	Blank
1088	Nov 01/93
1089	Blank
1090	Nov 01/93
1091	Blank
1092	Nov 01/93
1093	Blank
1094	Nov 01/93
1095	Nov 01/93
1096	Nov 01/93
1097	Nov 01/93
1098	Nov 01/93
1098.1	Nov 01/93
1098.2	Nov 01/93
1098.3	Nov 01/93
1098.4	Nov 01/93
1098.5	Nov 01/93
1098.6	Nov 01/93
1098.7	Nov 01/93
1098.8	Nov 01/93
1098.9	Nov 01/93
1098.10	Nov 01/93
1098.11	Nov 01/93
1098.12	Blank
1098.13	Blank
1098.14	Nov 01/93
1098.15	Blank
1098.16	Nov 01/93
1098.17	Nov 01/93
1098.18	Nov 01/93
1098.19	Nov 01/93
1098.20	Nov 01/93
1098.21	Nov 01/93
1098.22	Nov 01/93
1098.23	Nov 01/93
1098.24	Nov 01/93
1098.25	Blank
1098.26	Nov 01/93
1098.27	Nov 01/93
1098.28	Blank

PAGE	DATE

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

TABLE OF CONTENTS

TITLE PAGE

DESCRIPTION AND OPERATION 1
1. General 1
2. Packaging 1
3. Part Numbering 2
4. Specifications 3
5. Data and Program Modules 4
6. Signal Processing Boards 5
7. Power Supply 5
8. Backplane 5
9. Electromagnetic Interference (EMI) Filter 5
10. MKVII Software 5
11. Aircraft Configuration 6
12. MKVII Warning Computer Operation 6
A. Mode 1 Excessive Descent Rate Alert/Warning 7
B. Mode 2 Terrain Closure Rate Warning 7
C. Mode 3 Alert to Descent After Takeoff 8
D. Mode 4 Alert to Insufficient Terrain Clearance 9
E. Mode 5 Alert To Descent Below Glideslope 10
F. Mode 6 Altitude Callouts/Bank Angle 11
G. Mode 7 Windshear Detection 14
H. Windshear Recovery Guidance 19
I. Mark II Emulation Mode 19
J. Mode Switching 19
13. Theory of Operation 19
A. Program/Data Modules 20
B. Signal Inputs and Outputs 21
C. ADDA Board 21
D. PVM Board 44
E. Power Supply Board 68
F. Backplane Connectors 73
G. EMI Filter 73

TESTING AND TROUBLESHOOTING 101
1. General 101
2. Skill Level of Repair Technicians 101
3. Test Equipment 101
4. GSE Setup 101
5. GSE Power Requirements 101
6. Test Conditions 101

TABLE OF CONTENTS

TITLE	PAGE
7. Quality Assurance Provisions	102
8. GSE Malfunction/Failure	102
9. ATP Software Test Preparation	102
A. RS232 Communication Link Test (ATP and Diagnostics)	103
B. Configuration Test (ATP and Diagnostics)	103
C. Hardware Configuration Check (ATP and Diagnostics)	103
D. Flight Time Report (ATP and Diagnostics)	103
E. Fault Status Report (ATP and Diagnostics)	104
F. Flight History Check (ATP and Diagnostics)	104
G. Flight History Clearing (ATP Only)	105
H. NVM Clearing (ATP Only)	105
10. Acceptance Test Procedure (ATP)	106
11. Using the GSE System to Troubleshoot the MKVII	112
12. Troubleshooting the MKVII	113
13. Using the MKVII RS232 Terminal Interface	113
A. Powering the UUT	113
B. Terminal Interface Specification	125
C. Terminal Mode Initialization	125
D. PVM Command Interface	126
E. PVM Indirect Address Table	127
F. Special PVM Debugging Mechanisms	127
G. Digital-to-Analog Converter (DAC) Programming	127
H. Analog-to-Digital Converter (ADC) Read Back	127
I. ADDA Interface	127
J. ADDA Command Port Definition	127
K. ADDA Indirect Address Table	130
L. Special ADDA Debugging Mechanisms	131
14. Troubleshooting Examples	132
15. Memory Maps and Decoding Memory Devices	137
A. ADDA Memory Map	137
B. Output Equations	138
C. ADDA Gate Array (U53)	138
D. ADDA Gate Array Equations	139
E. PVM Memory Map	140
F. DECODER EQUATIONS	141
G. UART Signals	143
H. Interrupt Controller Signals	143
I. RAM Memory	143
J. Nonvolatile Memory	143

TABLE OF CONTENTS

TITLE PAGE

K. Dual Port RAM 143
L. Miscellaneous Input Buffer (address 5081H, NIO space, Read only) 144
M. Discrete Outputs (Address = 5001H, NIO Space, Write Only) 144
N. Mux Channels (Address = 50C1H, NIO Space, Write Only) 144

DISASSEMBLY 301
1. General 301
2. General Techniques 301
3. Warning Computer System 301

CLEANING 401
1. General 401
2. Cleaning Materials 401
3. Cleaning Procedures 401
A. Printed Wiring Board Assemblies 402
B. Connectors 402
C. Machined Metal Parts or Assemblies 402
D. Miscellaneous Metal Parts 403
E. Non-Metallic Parts 403

CHECK 501
1. General 501
A. Component Mechanical Checks 501
B. Component Electrical Checks 501

REPAIR 601
1. General 601
2. Solder 601
3. Wire 601
4. Finished Metallic Surfaces 601
5. Printed Wiring Board Assemblies 601
6. Electrostatic Discharge Service and Handling Information 602

ASSEMBLY (INCLUDING STORAGE) 701
1. General 701
2. General Techniques 701
3. Assembly Materials 701
4. A1 ADDA Board 701
5. A2 PVM Board 704
6. A3 Backplane Connector 707
7. A4 Power Supply Board 707
8. A7 EMI Filter 707
9. Storage After Assembly 708
A. Storage 708
B. Extended Storage 709

TABLE OF CONTENTS

TITLE	PAGE
FITS AND CLEARANCES	801
SPECIAL TOOLS, FIXTURES, AND EQUIPMENT	901
ILLUSTRATED PARTS LIST	1001
1. Introduction	1001
2. Definitions	1001
3. Equipment Designator Index	1002
4. Numerical Index	1002
5. Manufacturers' Codes, Names, and Addresses	1002
MANUFACTURERS CODE, NAME AND ADDRESS INDEX	1003
EQUIPMENT DESIGNATOR INDEX	1008
NUMERICAL INDEX	1033

LIST OF ILLUSTRATIONS

FIGURE	DESCRIPTION	PAGE
1	MKVII Warning Computer System	1
1A	Configuration Chart	2
1B	Warning Computer System Front Panel (-001 Shown)	3
2	Mode 1 Excessive Descent Alert and Warning Envelopes	7
3	Mode 2A Warning Envelope	8
4	Mode 2B Warning Envelope	9
5	Mode 3 Altitude Loss Alert Envelope	10
6	Mode 4A Minimum Terrain Clearance Alert Envelope	11
7	Mode 4B Minlmum Terrain Clearance Alert Envelope	12
8	Mode 4C Minimum Terrain Clearance Alert Envelope	13
9	Mode 5 Soft and Hard Alert Envelope	14
10	Bank Angle Warning Envelope, Program Module B01, B02, B03	15
10.1	Bank Angle Alert Threshold, Program Module B04 and on	16
11	Mode 6 Altitude Callouts	16
12	Mode 7 Block Diagram	17
13	Mode 7 Warning Envelope	18
14	MKVII Hardware Block Diagram	20
15	MKVII ADDA, PVM Signal Block Diagram	22
16	ADDA Functions Block Diagram	23
17	ADDA Board Memory	24
18	ADDA I/O Address Map	24
19	Discrete Input Port #1	25
20	Discrete Input Port #2	25
21	Discrete Input Port #3	26
22	ARINC 429 Transceiver Read Mode	27
23	ARINC 429 Transceiver Write Mode	27
24	429 Main Status Register	28
25	ARINC 429 Transmitter Control Register	29
26	ARINC 429 Transmitter Auxiliary Control Register	29
27	Output Data Latch #2	30
28	Output Data Latch #1	30
29	2-Wire Devices Input Address	31
3D	3-Wire Devices Input Address	32
31	Register Definitions	33
32	Program Pin Input Port #1	33
33	Program Pin Input Port #2	34
34	ADC Control Signals	38
35	PVM Block Diagram	45
36	Interrupt Control Scheme	48

LIST OF ILLUSTRATIONS

FIGURE	DESCRIPTION	PAGE
37	Interrupt Mask Register Bit Format	49
38	Interrupt Status Register Bit Format	49
39	Vector Interrupt Data	50
40	Miscellaneous Input Buffer	50
41	Discrete Outputs Data Bits	51
42	Voice Menu Words	53
43	Mux Channels, Address 50C1H	54
44	Identification Resistor Values	59
45	Power Supply Block Diagram	69
46	Backplane Pin-Outs	74
101	MKVII Test Equipment	102
102	MKVII WC Test Equipment Setup	103
103	Windows Program Manager	106
104	ATEasy Copyright Screen	107
105	ATEasy Password Dialog	107
106	Test Log Initial Information	108
107	ATEasy Control Window	108
108	GSE Master Configuration	109
109	Part Number Scroll Box	109
110	Voice Test Initial Dialog	110
111	Voice Test Conclusion Dialog	110
112	ATP Conclusion Test Log Screen	111
113	Test Log Print or Save Menu	111
114	Tasks and Tests	114
115	Program Profiles Choice	125
116	PVM Indirect Address Table	128
117	ADCDAT Table Organization	129
118	ADDA Command Word Table	130
119	ADDA Indirect Address Table	130
120	Analog and Digital Data Acquisition, 722-3514-001, A1	146
121	Analog and Digital Data Acquisition, 722-3514-002,004,006,008,010 A1	169
122	Analog and Digital Data Acquisition, 722-3514-005,007,009,011 A1	198.13
123	Analog and Digital Data Acquisition, 722-4024-030,031,035,036 A1	198.59
124	Processor/Voice/Memory, 722-3515-001,-002,-006,-007, A2	198.103
125	Processor/Voice/Memory, 722-3515-008,-009,-010,-011, A2	198.123
126	Processor/Voice/Memory, 722-3515-030,-031,-032,-033, A2	198.155
127	Processor/Voice/Memory, 722-4029-001,-002,-030,-031 A2	198.187
128	Backplane Assembly, 722-3602-001, A3	198.219
129	Power Supply, 722-3588-001,-002,-003, A4	198.223

LIST OF ILLUSTRATIONS

FIGURE	DESCRIPTION	PAGE
130	Power Supply, 722-3588-004,-005,-030,-031, 722-4080-003/004, A4	198.231
131	Filter, EMI, 716-0211-001,-002, A7	198.243
132	Analog and Digital Oata Acquisition, 722-4061-003, A1	198.245
133	Integrated Circuit Diagrams	198.289
401	Cleaning Materials	401
701	Repair Materials	602
701	Assembly Materials	702
702	C121/C122 Capacitor Replacement	703
703	C122/C123/C124 Capacitor Replacement	705
704	R237/R240/R241 Resistor Network Replacement	706
705	C37,39,41 thru 45 Lead Forming	707
706	R1 Installation	708
707	Shipping Parts	709
801	Fits and Clearances	801
901	Special Tools, Fixtures and Equipment	901
IPL 1	Mark VII Warning Computer System	1046
IPL 1A	Computer Subassembly	1052
IPL 2	Analog-Digital Data Acquisition, A1	1060
IPL 3	Processor/Voice/Memory, A2	1088
IPL 4	Backplane Assembly, A3	1098.10
IPL 5	Power Supply, A4	1098.14
IPL 6	Filter, EMI, A7	1098.26

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

INTRODUCTION

This manual has been prepared by Sundstrand Data Control, a Division of Sundstrand Corporation, according to ATA Specification No. 100.

The front matter consists of a title page that displays the equipment name and part number, and the ATA and document numbers assigned to the manual, a Record of Revisions page for recording revision incorporation, a Record of Temporary Revisions page for recording temporary revision (yellow page) insertion prior to formal revision, a Service Bulletin List that includes a brief description of the reason for the bulletin, and the date that Service Bulletin information was incorporated into the manual, a Table of Contents, and a List of Illustrations.

DESCRIPTION AND OPERATION section contains an equipment illustration, table of leading particulars, a general description, and a theory of operation for the electronic assemblies to assist in understanding the circuitry for fault isolation purposes.

TESTING AND TROUBLESHOOTING section contains a functional test to enable maintenance personnel to assess the operational condition of the equipment, calibration procedures for electronic or mechanical adjustment as necessary, troubleshooting guide to assist in fault isolation, and complete electrical wiring and schematic diagrams.

DISASSEMBLY section contains procedures for disassembling the equipment to the part replacement level. Complete overhaul procedures are not provided. Specific procedures are intended to be a supplement to, and are correlated to, the Illustrated Parts List *(IPL)*.

CLEANING section contains general cleaning procedures, which should be observed during repair and/or part replacement where applicable.

CHECK section contains general areas to visually observe during disassembly and assembly to assure that equipment operational standards are met.

REPAIR section contains specific instructions for repairing areas of the equipment not specifically covered in the ASSEMBLY section.

ASSEMBLY section contains all specific instructions necessary for part replacement and to supplement the *IPL*. Special instructions for use of adhesives, wires, heat sink compounds, etc., not covered in the *IPL*, are included. Special assembly sequence requirements, as applicable, are provided.

FITS AND CLEARANCES section contains a list of dimensional values, torques, etc., if required during assembly. These parameters are also specified in the ASSEMBLY section where applicable.

SPECIAL TOOLS, FIXTURES, AND EQUIPMENT section contains a list of all equipment required to perform procedures specified in the other manual sections.

ILLUSTRATED PARTS LIST *(IPL)* section contains illustrations and parts lists for all equipment assemblies, subassemblies, and components. The illustrations and parts lists are item-number keyed for location of parts, and list quantities, part numbers, and part descriptions. An introduction to the *IPL* relates how it is used, definitions used, equipment designators, and alphanumerical indices for parts.

VERIFICATION

Testing and Fault Isolation	Analysis	Dec 1/92
Disassembly	Analysis	Dec 1/92
Assembly	Analysis	Dec 1/92

APPREVIATIONS	DEFINITION
AC	Alternating current
AC/DC	AC-to-DC volts converter
ADC	Analog-to-digital converter
ADDA	Analog/digital data acquisition board
ADI	Attitude director indicator
AGL	Above ground level
AOA	Angle of attack
ARINC	Aeronautical Radio, Inc.
ARINC 429	Specification for DITS
ARINC 542	Specification for analog flight data acquisition
ARINC 404	Specification for ground proximity warning system
ASL	Above sea level
ATC	Air traffic control
ATL	Abbreviated test language for all systems
ATP	Acceptance test procedure
ATR	Air transport rated
BARC	Baro rate computer
BARO	Barometric
BIT	Built-in-test
BITE	Built-in-test equipment
BNR	Binary
BOB	Breakout box (test device)
BZW	Byte/word (active low)
CMM	Component maintenance manual
CPU	Central processing unit
CW	Change word
DAC	Digital-to-analog converter
DADS	Digital air speed system
dB	Decibels
DC	Direct current
DH	Decision height
DITS	Digital information transmission system
DM	Data module
DMM	Digital multimeter
DPR	Dual Port RAM
DW	Display word
EEPROM	Electronically erasable programmable read only memory
EMI	Electromagnetic interference
EOC	End of conversion
EOT	End of track
EPLD	Erasable programmable logic device
ESD	Electrostatic sensitive device
FD	Flight director
FPM	Feet per minute
ft	Feet
ft/sec	Feet per second
GND	Ground electrical return
GPIB	General purpose interface bus
GPWC	Ground proximity warning computer
GPWS	Ground proximity warning system

APPREVIATIONS	DEFINITION
GS	Ground speed
GSE	Ground support equipment
GSU	Guidance switching unit
Hz	Hertz
IAS	Indicated air speed
IB	Input byte
ILS	Instrument landing system
INOP	Inoperative
INT	Interrupt
I/O	Input/output
IPL	Illustrated parts list
kHz	Kilohertz
Kts	Knots per hour
LRU	Line replaceable unit
LSB	Least significant bit
LSC	Least significant character
mHz	Megahertz
MKVII	Mark seven warning computer
MSB	Most significant bit
NAND	Not AND gate
NMI	Non-maskable interrupt
NOR	Not OR gate
NVM	Nonvolatile memory
OB	Output byte
OEM	Original equipment manufacturer
PC	Personal computer
PM	Program Module
P/N or PN	Part number
PVM	Processor/voice/memory board
PWB	Printed wiring board
PWR	Power
QFE	Local station pressure
RA	Radio altitude
RAM	Random access memory
RCVR	Receiver
RD	Read Memory
REPLS	Replaces
ROM	Read only memory
RST	Reset
R/W	Read/write
RW	Write to memory
RX	Receiver
SAT	Static air temperature
Sec	Second
SH	Sheet
SM	Surface mount
S/N or SN	Serial number
TAS	True air speed
TCAS	Traffic alert and collision avoidance system
T/O	Takeoff

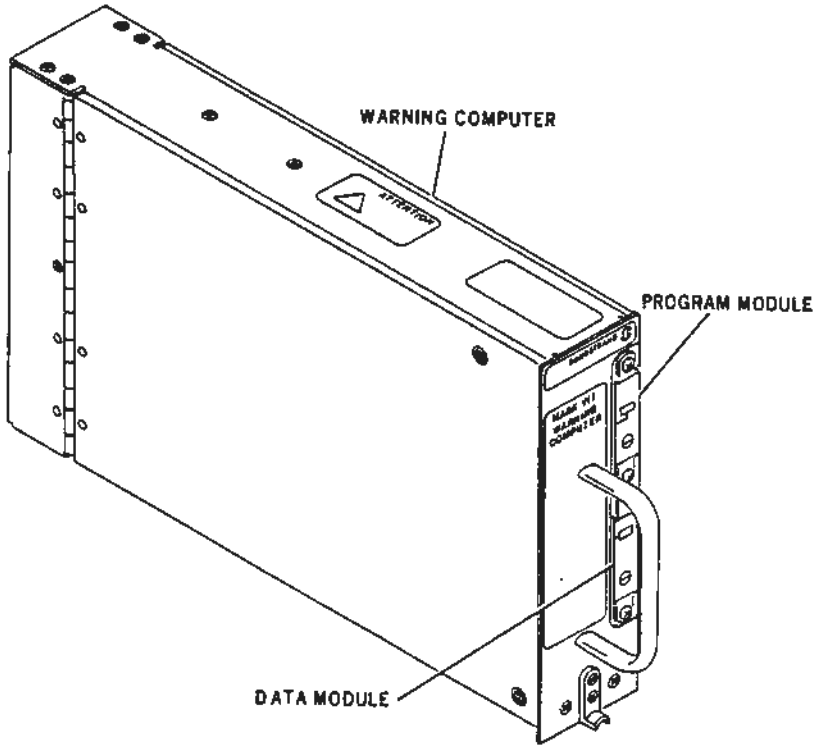
APPREVIATIONS	DEFINITION
TOGA	Take off go around
TSO	Technical Standard Order
TX	Transmit
UUT	Unit under test
VAC	Volts alternating current
VDC	Volts direct current
VLSI	Very large scale integration
WC	Warning computer
WDOG	Watchdog
WE	Write enable
W/O	Without
WS	Windshear
XCVR	Transceiver
XMTR	Transmitter

COMPONENT MAINTENANCE MANUAL
PART NO. 960-0284

DESCRIPTION AND OPERATION

1. General

The Warning Computer System (MKVII) is a digitally controlled computer that provides ground proximity alerts and optional windshear detection. The MKVII can also provide recovery guidance during a windshear condition. Aural and visual alerting is provided for ground proximity warning system (GPWS) warnings, and aural annunciations are provided for altitude and bank angle callouts. In the event of a severe windshear encounter, alerting is provided to the pilots in the form of visual and aural annunciations, and windshear recovery pitch and roll commands can be displayed on the aircraft attitude director indicator (ADI). A Technical Standard Order (TSO) is required for installation of the MKVII on any type of aircraft. Figure 1 shows the front view of the MKVII Warning Computer System.



MKVII Warning Computer System
Figure 1

2. Packaging

The MKVII is housed in a 1/4 ATR (air transport rated) enclosure. Its connector configuration is designed to be compatible with existing ARINC (Aeronautical Radio, Inc.) 594 GPWS wiring. The unit is coated with a textured blue color semigloss paint, except for the bottom surface, which is unpainted chromate conversion coated aluminum. The unit is marked in accordance with the requirements of ARINC 594.

The warning computer system consists of the MKVII warning computer (WC), data module, and program module. Figure 1A gives the warning computer system part numbers covered in this manual and the corresponding warning computer, data module, and program module part numbers. The WC has five subassemblies: Analog/Digital Data Acquisition Board (ADDA), Processor/Voice/Memory Board (PVM), Power Supply Board, Backplane, and Electromagnetic Interfer-

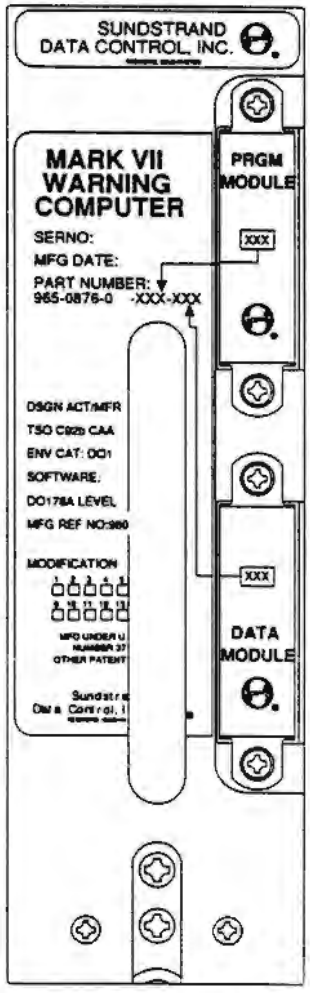
WARNING COMPUTER SYSTEM	WARNING COMPUTER	PROGRAM MODULE	DATA MODULE
960-0284-001	965-0876-001-A01-A01	964-0406-001	964-0407-001
960-0284-003	965-0876-001-B01-B01	964-0406-002	964-0407-003
960-0284-004	965-0876-001-B01-B02	964-0406-002	964-0407-004
960-0284-005	965-0876-001-B02-B02	964-0406-003	964-0407-004
960-0284-006	965-0876-001-B01-B03	964-0406-002	964-0407-005
960-0284-007	965-0876-001-B02-B03	964-0406-003	964-0407-005
960-0284-008	965-0876-001-B03-B03	964-0406-004	964-0407-005
960-0284-009	965-0876-001-B03-B04	964-0406-004	964-0407-006
960-0284-010	965-0876-001-B04-B04	964-0406-005	964-0407-006
960-0284-011	965-0876-001-B04-B03	964-0406-005	964-0407-005
960-0284-012	965-0876-001-B04-B05	964-0406-005	964-0407-007
960-0284-013	965-0876-001-B04-B06	964-0406-005	964-0407-008
960-0284-014	965-0876-001-B03-B06	964-0406-004	964-0407-008
960-0284-015	965-0876-001-B05-B01	964-0406-006	964-0407-003
960-0284-016	965-0876-001-B05-B02	964-0406-006	964-0407-004
960-0284-017	965-0876-001-B05-B03	964-0406-006	964-0407-005
960-0284-018	965-0876-001-B05-B04	964-0406-006	964-0407-006
960-0284-019	965-0876-001-B05-B06	964-0406-006	964-0407-008
960-0284-020	965-0876-001-B06-B04	964-0406-007	964-0407-006
960-0284-021	965-0876-001-B06-B06	964-0406-007	964-0407-008
960-0284-030	965-0876-030-B03-B03	964-0406-004	964-0407-005
960-0284-031	965-0876-030-B03-B04	964-0406-004	964-0407-006
960-0284-032	965-0876-030-B04-B04	964-0406-005	964-0407-006
960-0284-033	965-0876-030-B04-B03	964-0406-005	964-0407-005
960-0284-034	965-0876-030-B04-B05	964-0406-005	964-0407-007
960-0284-035	965-0876-030-B04-B06	964-0406-005	964-0407-008
960-0284-036	965-0876-030-B03-B06	964-0406-004	964-0407-008
960-0284-037	965-0876-030-B05-B03	964-0406-006	964-0407-005
960-0284-038	965-0876-030-B05-B04	964-0406-006	964-0407-006
960-0284-039	965-0876-030-B05-B05	964-0406-006	964-0407-007
960-0284-040	965-0876-030-B05-B06	964-0406-006	964-0407-008
960-0284-041	965-0876-030-B06-B04	964-0406-007	964-0407-006
960-0284-042	965-0876-030-B06-B06	964-0406-007	964-0407-008

Configuration Chart
Figure 1A

ence (EMI) Filter.

3. **Part Numbering**

The basic operational capabilities of the MKVII are determined by the 16-digit part number identified on the front panel (refer to Figure 1B). The first seven digits, 965-0876, identify the computer as part of the MKVII family and are the same for all MKVII systems. The next three numbers, 001 or 030, identify the internal hardware version. Minor hardware revisions are identified on the modification status block on the front panel. The last six digits of the part number are the revision numbers of the replaceable front panel program and data modules. Replacement of either module automatically updates the MKVII part number to reflect the new system configuration.



Warning Computer System Front Panel (-001 Shown)
Figure 1B

4. **Specifications**

The MKVII conforms to the environmental requirements of the following specifications.

A. Temperature

Category: A2

```
High Temperature - Nonoperating:  +85° C
High Temperature - Operating:  +70° C
Low Temperature - Operating:  -25° C
Low Temperature - Nonoperating:  -55° C
```

B. Temperature Variation

Category: B 5.0°C/Minute

C. Humidity

Category: A +55°C maximum Temperature

D. Electromagnetic Interference

Magnetic Effect, Category: Z

E. Power Input

Category: A

F. Voltage Spikes

Category: A

G. Audio Frequency Conducted Susceptibility

Category: A

H. Induced Signal Susceptibility

Category: Z

I. Radio Frequency Susceptibility

Category: Z

J. Emission of Radio Frequency Energy

(1) Conducted - Category: Z

(2) Radiated - Category: B

K. Lightning Induced Transient Susceptibility

Category: J and K

L. Weight

The unit maximum weight shall not exceed 6.0 pounds.

M. Power Requirement

115 Vac, 400 Hz single-phase 28 volts DC [for lights and guidance switching unit (GSU) as required].

N. N. Power Dissipation

```
13 watts maximum with no warnings
16 watts with warnings and 8-ohm speaker connected
(Power dissipation will increase by 1.5 watts maximum
while powering the biaxial accelerometer unit and by
1.2 watts maximum while powering an airspeed transducer.)
```

5. **Data and Program Modules**

The data and program modules are installed in the front panel of the WC. The program module contains the functional algorithms. The data module (DM) contains the data tables allowing the

WC to be configured to operate with a variety of interfaces in large commercial aircraft.

The program module contains 64K bytes of read only memory (ROM). The ROM memory contains the encoded instructions and software for programming operation of the PVM microprocessor.

The data module consists of 64K bytes of ROM. This module contains aircraft specific data and scaling parameters which allow the WC to interface with a variety of sensor types and aircraft configurations.

6. **Signal Processing Boards**

The ADDA board contains software, memory, an 80186 microprocessor, analog-to-digital converters, and associated hardware. Many of the components are surface mount packaging, which permits the MKVII to provide multiple modes of alert/warnings in the unit.

Through the MKVII rear panel backplane, the ADDA board acquires analog, digital, and discrete data from the aircraft sensors. The ADDA uses configuration data from the PVM to develop scaled digital sensor data which the ADDA sends to the PVM to be used to output warnings and recovery guidance signals. The ADDA also performs redundant computations of certain recovery guidance functions for checking the PVM recovery guidance calculations. The ADDA communicates with the PVM through the dual port random access memory (RAM) (DPR) memory on the PVM board.

The PVM contains software, memory, a Z8002 microprocessor, and associated hardware. The PVM filters scaled input data, determines alerting boundary penetrations, and issues the visual and aural alert signals and recovery guidance information signals while the host aircraft is in an alerting envelope.

7. **Power Supply**

The power supply converts aircraft supplied 115Vac, 400 Hz power to ±14Vdc, ±12Vdc, and +5Vdc used in the GPWC. ±24Vdc produced by the MKVII powers two external sensors. The power supply also powers various sensor devices on the aircraft (depending on the installation requirements).

8. **Backplane**

The backplane interfaces the aircraft inputs/outputs to the WC.

Program pins are a specified group of backplane input pins in connectors J1A and J2. The MKVII uses the program pins to identify aircraft configuration and modes of operation the customer specifies. They are discrete-type inputs. At the first time the WC has power applied while on a particular aircraft, the program pins information is placed in PVM nonvolatile memory (NVM). The remaining backplane inputs/outputs are assigned to be compatible with ARINC 429 specifications. Figure 46 in this section of the manual provides pin assignments on the backplane.

9. **Electromagnetic Interference (EMI) Filter**

The EMI filter provides spike protection to the WC. The power input to the WC from the aircraft power plant is 115Vac, 400 Hz. The EMI removes unwanted DC voltage spikes using L1 and L2. C1 and C2 remove AC spikes. FL1 and FL2 act as 115Vac plus (+) and minus (-) fuses to open in the event of a current spike input from the aircraft of more than 125Vac.

10. **MKVII Software**

The software is developed to the standards of DO-178A, Level 2 requirement. The ADDA software is written in 80186 assembly language. It uses modular implementation of a system for database control of the interface hardware. The interface is set up by the PVM software using data retrieved from the aircraft configuration database according to WC program pins.

The PVM software is written in Z8002 assembly language. It uses modular implementation con-

sisting of the operating system, warning computer high level functions, and built-in-test (BIT) functions. The PVM software is contained in the front panel program and data modules.

The ADDA, PVM, PM, and DM software are programmed in assembly language. The microprocessor for the PVM is a Zilog Z8002 and it operates at 6mHz clock. The microprocessor for the ADDA is an Intel 80186 operating at 8mHz. The data the ADDA needs to preserve is stored in the PVM RAM.

Aircraft input signal data and the reference inputs are configured on the same channel but use different analog-to-digital converters (ADC). Both the data and the reference can be collected at the same time. Only binary (BNR) ARINC 429 serial bus data is processed, no ARINC 429 (BCD) information is processed.

11. **Aircraft Configuration**

NOTE: The conditions and tests required for TSO approval of this article are minimum performance standards. It is the responsibility of those desiring to install this article either on or within a specific type of class of aircraft to determine that the aircraft installation conditions are within the TSO standards. The article may be installed only if further evaluation by the applicant documents an acceptable installation and is approved by the Administrator.

The MKVII is designed to be used on various aircraft which use different sensor devices and wiring schemes. To provide such flexible interface, program pin inputs are used to tell the WC what configuration of aircraft it is installed on. These program pins also identify the interface characteristics or customer options being used.

With the MKVII in the aircraft, after a successful power up test, the ADDA samples the program pin inputs and sends the data to the PVM through the DPR. The PVM then extracts the configuration data from the data module. The data module information on where a particular signal is coming in (which physical input pins), or electrical characteristics, and scaling routines for input signals is passed from the PVM to the ADDA. The ADDA then manipulates the sensor input signals using the configuration specific parameters. During the configuration data transfer between the PVM and the ADDA, the memory location for UNCONFIGURED is set to 1. When the transfer of data is complete, UNCONFIGURED is set to 0. This boolean UNCONFIGURED information is used by the input signal processors to determine if the input data is from the correct source and that it is scaled properly.

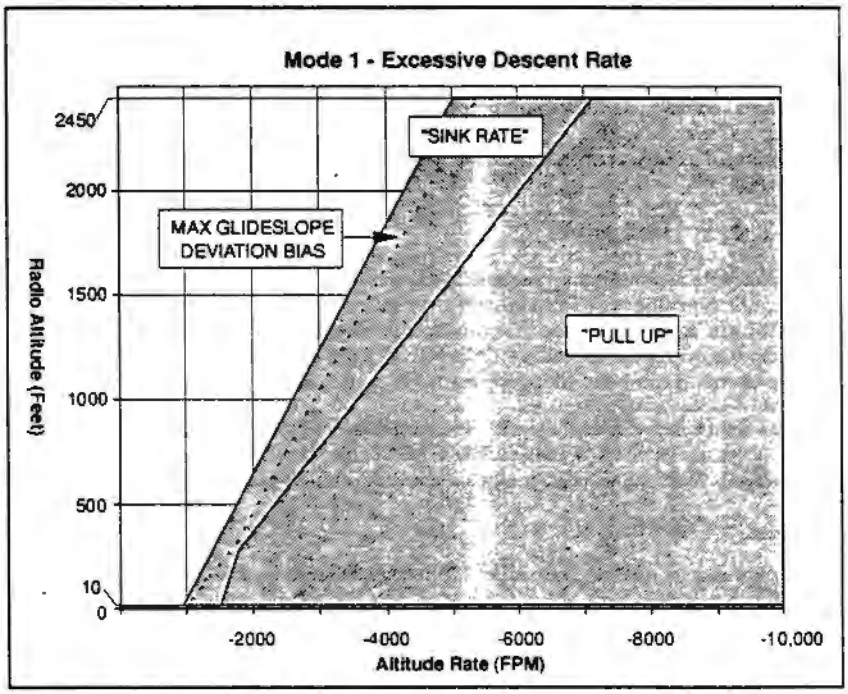
The configuration database, consisting of an index-structured hexadecimal database containing all information required by the PVM software to configure the MKVII automatically on power up for a variety of aircraft installation types, is stored in the memory of the data module.

12. **MKVII Warning Computer Operation**

The MKVII is designed to be compatible with aircraft using analog input sensors and can support four channels of ARINC 575 and 429 digital input signals. In most cases of installation, existing aircraft sensors are used.

The MKVII performs the following types of functions:

- ***Ground Proximity Warning System***
- ***Altitude Callouts and Bank Angle Warnings***
- ***Windshear Detection and Alerting***
- ***Windshear Recovery Guidance (Optional)***
- ***Self Test and System Fault Monitoring***



Mode 1 Excessive Descent Alert and Warning Envelopes
Figure 2

In order to have the MKVII provide complete coverage of ground proximity circumstances, seven modes of warnings are available in a priority scheme that meets or exceeds FAA requirements. An optional audio reduction reduces alert repetitions.

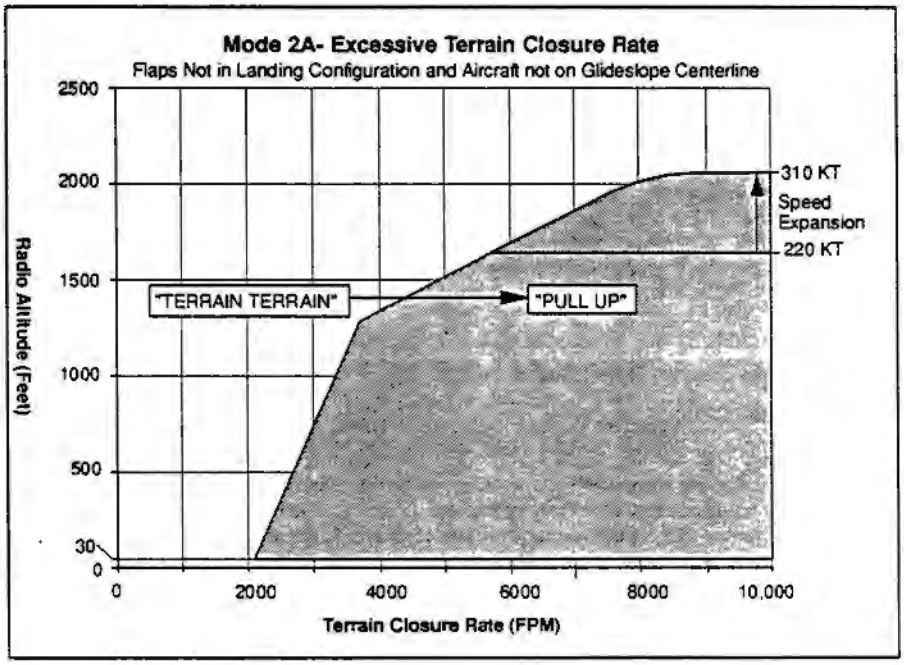
Several of the seven modes of operation are divided into **submodes** to produce individual flight circumstance alert/warnings. No two modes can be annunciated at the same time in order to provide the flight crew with circumstance priority alert/ warnings that cannot contradict safety procedures. The following information lists and describes each mode.

A. **Mode 1 Excessive Descent Rate Alert/Warning**

Mode 1 provides alert/warning for high descent rates into terrain. When the alert envelope is penetrated, the message **SINK RATE** will annunciate and the GPWS alert lamps will light. The message **WHOOP WHOOP PULL-UP** will occur when the warning envelope is penetrated. The descent rate required to cause a **SINK RATE** to occur is automatically increased if the pilot is safely repositioning down from slightly above the glideslope centerline. Figure 2 shows a graph of the excessive descent alert and warning envelopes.

B. **Mode 2 Terrain Closure Rate Warning**

Mode 2 provides two submodes of alert/warnings to help aircraft avoid striking the ground when the terrain is rising too fast with respect to the aircraft. Mode 2 provides warnings based on radio altitude (height above ground) and on how rapidly that radio altitude is decreasing. The warning envelope is adjusted depending on aircraft configuration and speed.



Mode 2A Warning Envelope
Figure 3

(1) Mode 2A

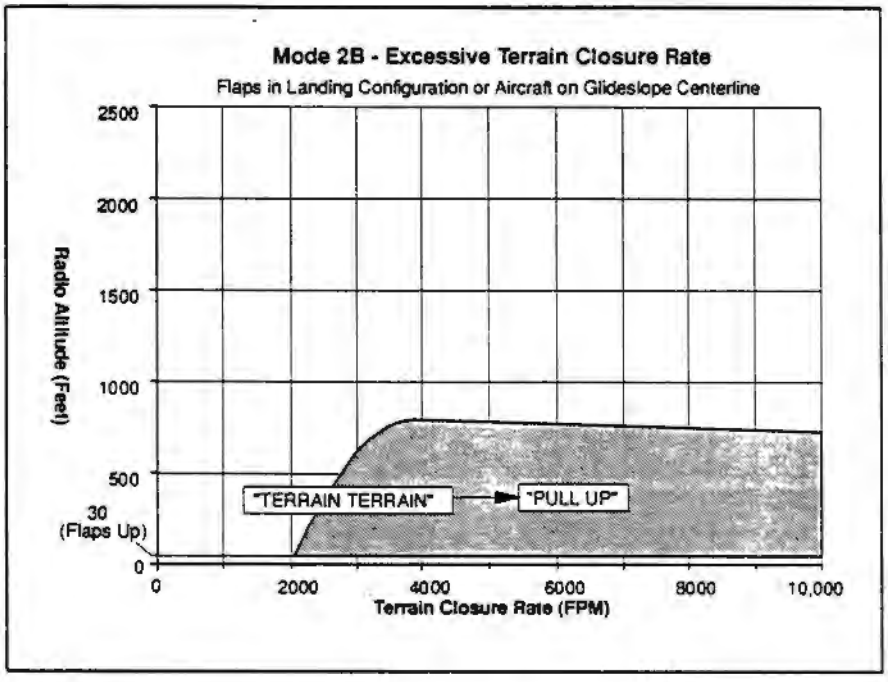
Mode 2A is active when flaps are not in a landing position and the aircraft is not on an instrument landing system (ILS) approach with a glideslope deviation less than ±2 dots. Figure 3 shows a typical warning envelope for Mode 2A. In Mode 2A, the **TERRAIN TERRAIN** message occurs once and the GPWS alert lamps light when the alert envelope is penetrated (the aircraft is approaching the terrain too quickly). If the envelope penetration persists, the warning **WHOOP WHOOP PULL-UP** will occur repetitively. The **PULL-UP** warnings will cease when the envelope is exited. Normally the message **TERRAIN** will then start and repeat until 300 feet of barometric altitude is gained. If the warning envelope is reentered before the **TERRAIN** messages are terminated, a single **TERRAIN-TERRAIN** will occur, followed by the repetitive **WHOOP WHOOP PULL-UP** annunciation.

(2) Mode 2B

Mode 2B is active whenever flaps are in a landing position or when the aircraft is performing an ILS approach and the glideslope deviation is less than ± 2 dots. Figure 4 shows a typical warning envelope for Mode 2B. When the alert envelope of Mode 2B is penetrated, the message **TERRAIN-TERRAIN** will occur and the alert lamps will light. If flaps or gear are up, a **WHOOP WHOOP PULL-UP** will sound when the previous message is complete. However, with flaps and gear down, a repetitive **TERRAIN** will be annunciated. Both repetitive voices will cease, and the alert lamps will extinguish, when the envelope is exited.

C. **Mode 3 Alert to Descent After Takeoff**

Mode 3 provides alerts for excessive altitude loss after takeoff, or after a go-around from below 245 feet above ground level (AGL). When the Mode 3 alert occurs, the voice message **DON'T**



Mode 2B Warning Envelope
Figure 4

SINK is given and the ground proximity warning lamp(s) are lit.

The Mode 3 alert is based on barometric altitude loss and radio altitude sensor inputs. A biasing, or desensitizing of the envelope occurs with time elapsed since the initiation of takeoff/go-around. Figure 5 shows a graph of the Mode 3 altitude loss alert envelope.

D. **Mode 4 Alert to Insufficient Terrain Clearance**

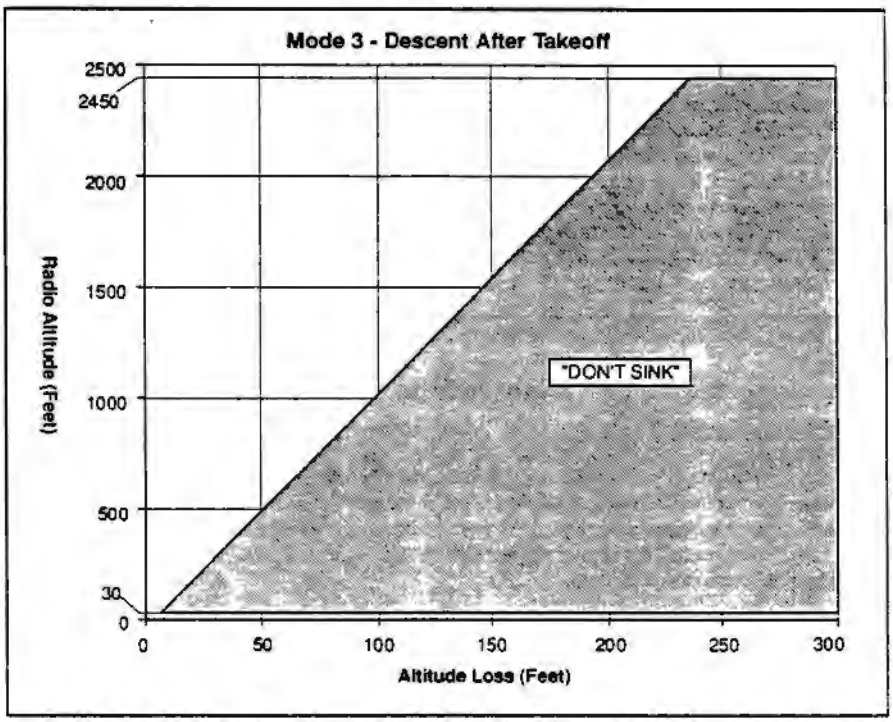
Mode 4 generates three types of alerts based on radio altitude, airspeed, and flight mode. These are referred to as Modes 4A, 4B, and 4C. Mode 4A is active during cruise and approach with landing gear up. Mode 4B is active during cruise and approach with landing gear down and flaps up. Mode 4C is active during a takeoff. Warnings from Modes 4A, 4B, and 4C cannot occur at the same time.

(1) Mode 4A

A Mode 4A alert occurs when its respective envelope is penetrated with airspeed less than or equal to 190 Kts. The alert lamps light and the message **TOO LOW GEAR** annunciates when this occurs. This message repeats until either the envelope is exited, which causes the voice to cease and the alert lamps to extinguish, or airspeed exceeds 190 Kts, which causes the **TOO LOW TERRAIN** message to occur repetitively. Figure 6 shows a graph of Mode 4A minimum terrain clearance alert envelope.

(2) Mode 4B

Mode 4B occurs when the Mode 4B alert envelope is penetrated. The warning lamps light, and one of three different voice alerts occurs, depending on the situation. If flaps are up and the gear is down with the airspeed less than 160 Kts, the **TOO LOW FLAPS** message repeats. If the gear is up with the airspeed less than 160 Kts, the **TOO LOW GEAR** message



Mode 3 Altitude Loss Alert Envelope
Figure 5

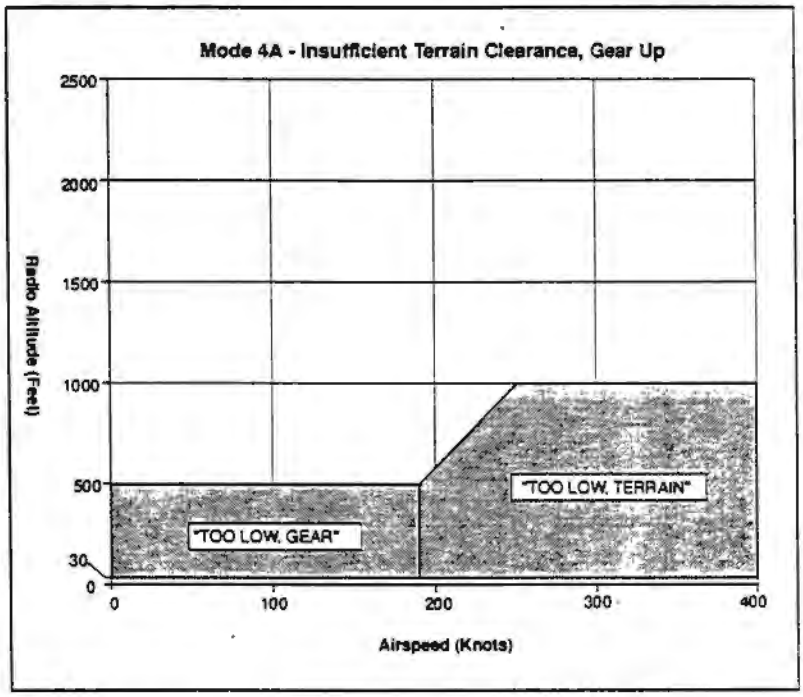
repeats. If the airspeed is greater than 160 Kts when the envelope is penetrated, the **TOO LOW TERRAIN** message repeats. Figure 7 shows a graph of the Mode 4B minimum terrain clearance alert envelope.

(3) Mode 4C

Mode 4C is based on a minimum terrain clearance, or floor, that increases with radio altitude during takeoff. This floor is at 3/4 of the highest value of radio altitude that has occurred during takeoff phase of flight. The Mode 4C floor generator is enabled at 100 feet of radio altitude on takeoff, and continues until the approach phase of flight is activated, or until the radio altitude decreases below 30 feet. If a go-around is being performed, the altitude at which the warning floor is enabled is 245 feet. The floor value is conditioned, so that it is not affected by small irregularities in terrain, to reduce nuisance warnings. The floor is not allowed to decrease. If the floor is penetrated, which will occur if the aircraft starts a descent during takeoff, or if the terrain rises beneath the aircraft at a steeper gradient than the aircraft is climbing, the **TOO LOW TERRAIN** aural message repeats until the aircraft has gained sufficient clearance from the terrain. Figure 8 shows a graph of the Mode 4C minimum terrain clearance alert envelope.

E. **Mode 5 Alert To Descent Below Glideslope**

Mode 5 provides alerts for excessive glideslope deviation when the aircraft descends below the glideslope beam on front-course ILS approach. Two audio volume levels of alerts are available, depending on the severity of the glideslope deviation condition. The low volume level warning is referred to as the **soft** alert, and is annunciated -6dB below the normal warning volume. The normal volume level warning is referred to as the **hard** alert. Figure 9 shows the Mode 5 soft and hard alert envelope.



Mode 4A Minimum Terrain Clearance Alert Envelope
Figure 6

F. **Mode 6 Altitude Callouts/Bank Angle**

Mode 6 provides optional callouts that are annunciated as the aircraft descends through predefined altitudes below 2500 feet AGL or through the decision height set by the pilot on the radio altimeter. Mode 6 can also provide aural alert of excessive aircraft bank angle. Selection by program pins (32 possible menus) determines which Mode 6 callouts are enabled in an installation.

(1) Bank Angle Callout

The optional bank angle function provides an aural warning based on aircraft roll angle, radio altitude, and altitude rate. The bank angle option is enabled as part of the Mode 6 menu selection and is active for all phases of flight, including cruise.

(a) Program Modules B01, B02, B03

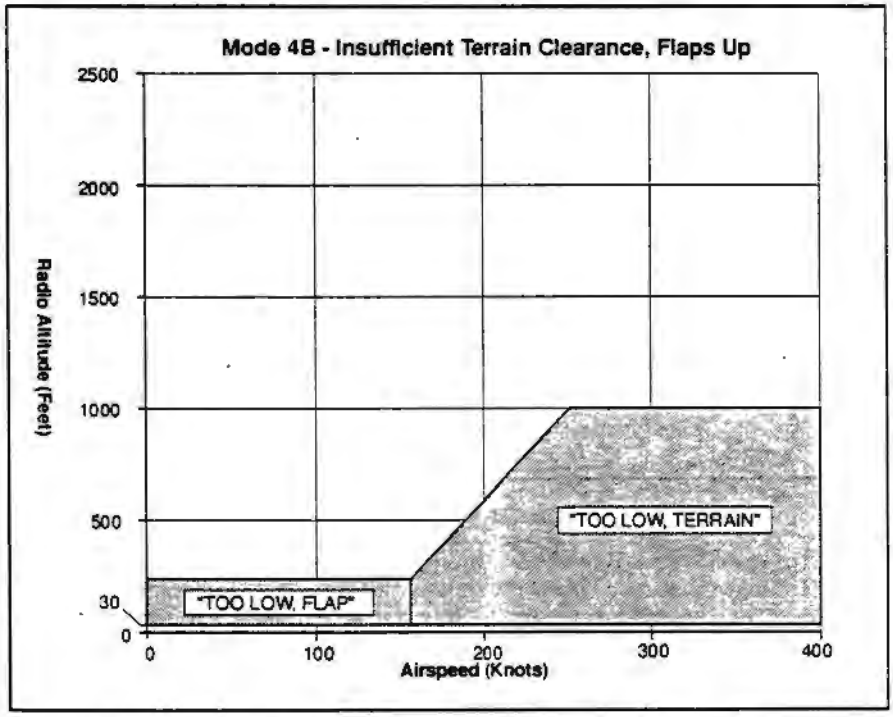
Figure 10 shows the bank angle warning envelope. This curve is divided into two sections. The first is active below 300 feet AGL and generates warnings based on roll, roll-rate, and radio altitude. The warning is based on the following equation:

Roll Angle (^{O}) = Radio Altitude (ft) x 0.113333 (^{O})/ft) + 6 (^{O})

... where roll angle is the warning threshold for the particular radio altitude.

This warning threshold is decreased by 1.5^{O} for every 1^{O} per second of roll rate. This advancement is limited to 6^{O} and is only active when roll attitude is greater than 5^{O}.

Above 300 feet AGL, the warning threshold is determined by the following equation:



Mode 4B Minimum Terrain Clearance Alert Envelope
Figure 7

Roll Angle (^{O}) =

$$\frac{-240\ (^{O}/sec) \times \text{Radio Altitude (ft)} - 137{,}280\ (ft^{O}/sec)}{(^{O})\ \text{Altitude Rate (ft/sec)}} - 142.4^{O}$$

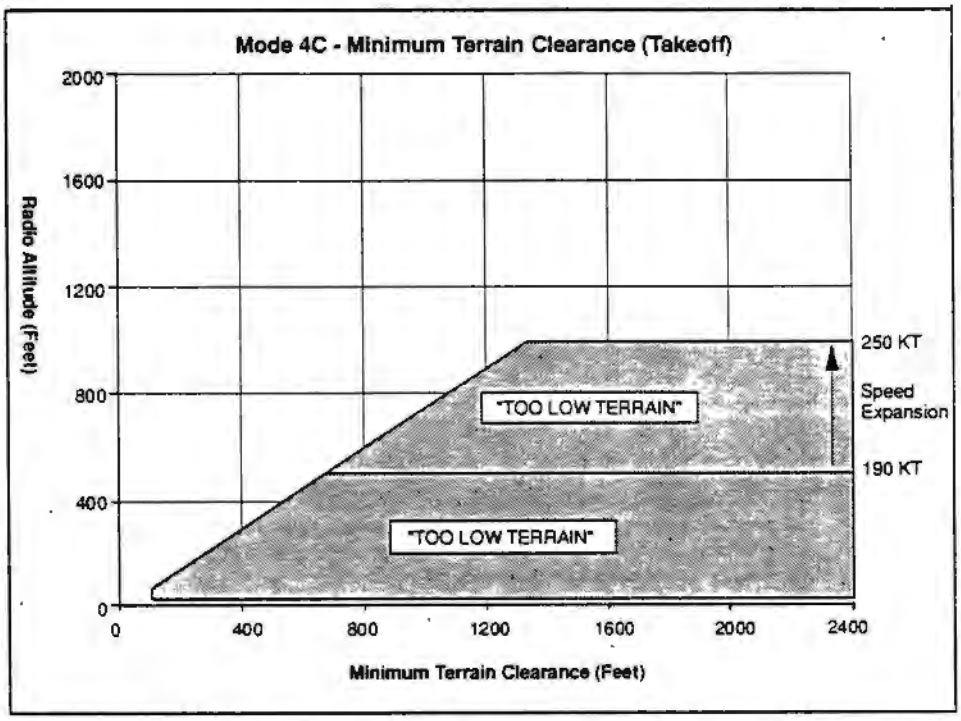
... where roll angle is the warning threshold for the particular radio altitude and altitude rate.

The output of this equation is decreased by 1.5^{O} for every 1^{O} per second of roll rate. This advancement is limited to 6^{O}. The warning threshold above 300 feet is also limited such that an alert will never be generated for bank angles less than 31^{O} and will always be generated for bank angles greater than 40^{O}. If radio altitude is invalid, the warning threshold defaults to 40^{O}. The bank angle envelope continues to be calculated when the radio altitude is out of track, providing bank angle protection at all aircraft altitudes.

Whenever the roll angle exceeds the warning thresholds described in the previous paragraphs, two **BANK ANGLE** warning voice messages are given. Two additional messages are generated if the roll angle increases by an additional 20%. If the roll exceeds 40% of the threshold, continuous **BANK ANGLE** warnings are generated. No visual warnings are generated for bank angle alerts.

(b) Program Modules B04 and on

In Program Modules B04 and later, the optional bank angle function provides an aural warning based on aircraft roll angle and radio altitude; neither roll rate nor descent rate affect the warning curve. The bank angle option is enabled either as part of the



Mode 4C Minimum Terrain Clearance Alert Envelope
Figure 8

Mode 6 menu selection, or, in non-MK II Emulation Mode installations, through the activation of the bank angle enable program pin. Figure 10.1 shows the bank angle warning envelope. This curve is divided into two sections. the first is active below 150 feet AGL and generates warnings based on roll and radio altitude. The warning is based on the following equation:

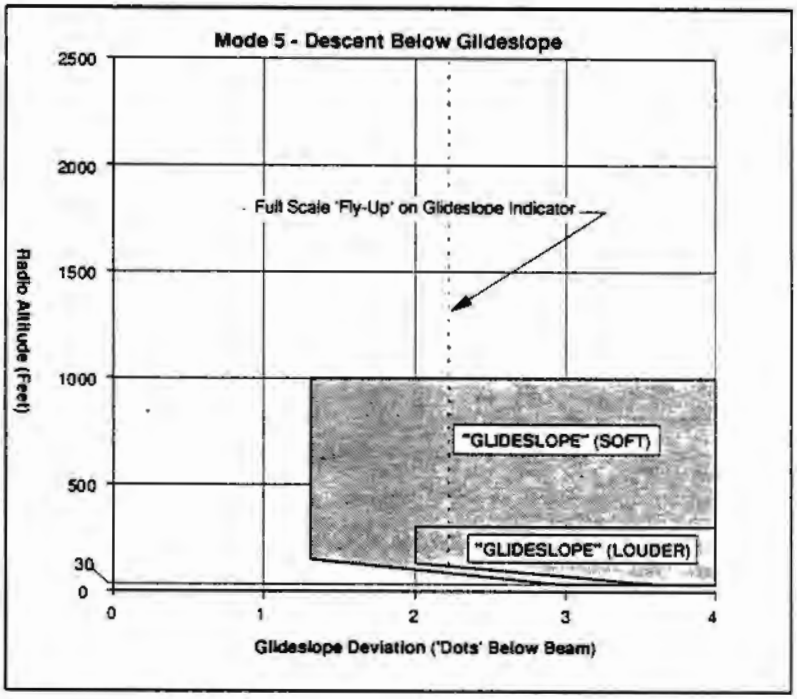
- ***Roll Angle (degs) = Radio Altitude (Ft) x 0.25 (Degs/Ft) + 2.5 (Degs)***

Where roll angle is the warning threshold for the particular radio altitude. Bank Angle warnings are not given at less than 10 degrees of roll angle or when radio altitude is below 5 feet. Above 150 feet, the warning threshold is 40 degrees (and is not a function altitude rate in Program Modules B04 and later).

Whenever the roll angle exceeds the warning thresholds as described above, two **BANK ANGLE** warnings voice messages are given. If radio altitude is greater than 150 feet, these two messages are separated by a 0.75 second pause; if radio altitude is less than 150 feet, there is no pause between the two messages. Two additional messages are generated if the roll angle increases by an additional 20%. If the roll exceeds 40% of the threshold, two **BANK ANGLE** messages are issued every three seconds (i.e., BANK ANGLE, BANK ANGLE, 3 second pause, BANK ANGLE, BANK ANGLE). No visual warnings are generated for bank angle alerts.

(2) Altitude Callouts

The standard altitude callouts available for inclusion in the Mode 6 menus are listed in Figure 11. Mode 6 altitude callouts are enabled when the MKVII transitions from takeoff to approach mode or the radio altitude exceeds 1000 feet and approach mode is active.



Mode 5 Soft and Hard Alert Envelope
Figure 9

When a callout is annunciated, a nonvolatile latch is set. This prevents the callout from repeating. A callout will not be repeated until the enabling logic has been set again.

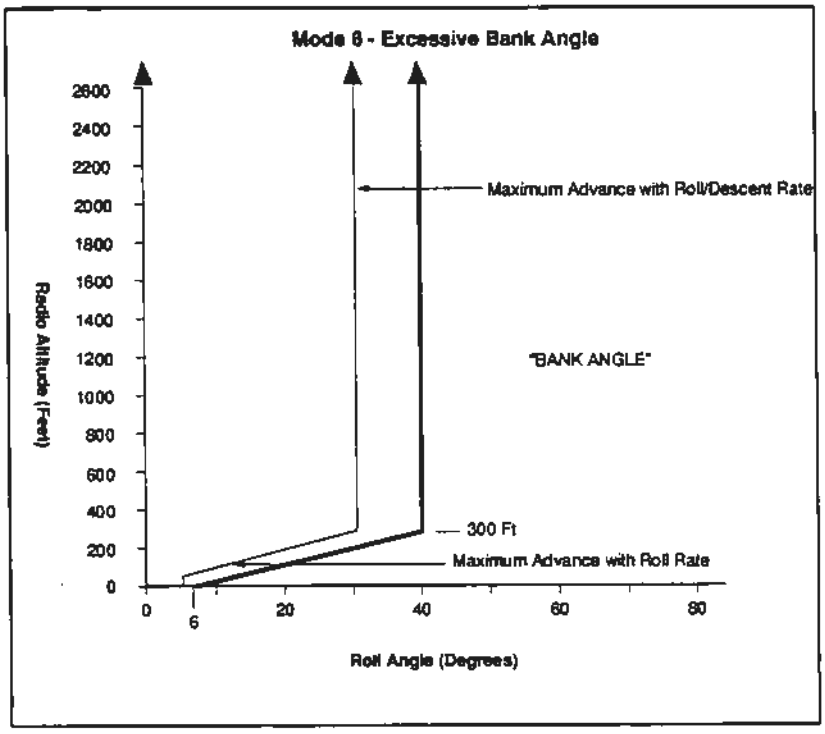
The standard altitude callouts (1000, 500, etc.) are only annunciated in a band between the associated value and at a value less than this value; defined as follows: If the current altitude is 150 feet or less, the band is 10 feet deep. If the altitude is greater than 150 feet, the band is 20 feet deep. If the callout is not issued in this band, the computer performs as though the callout was given, and the callout cannot be repeated until reset as described in the previous paragraph.

The **DECISION HEIGHT , MINIMUMS,** or **MINIMUMS-MINIMUMS** callout is annunciated once, for the first transition of the DECISION HEIGHT discrete encountered between 1000 and 30 radio altitude with landing gear down. This annunciation must occur within either 10 or 20 feet of the DECISION HEIGHT activation altitude in a fashion similar to the altitude callouts described in the previous paragraph.

A 'smart' 500-foot callout is available to provide timely alert of a possible inadvertent descent. When the 'smart' 500-foot callout is enabled, the callout **FIVE HUNDRED** is annunciated as the aircraft descends through 500 feet only if ILS is not selected or glideslope is not within 2.0 dots of the beam centerline.

G. Mode 7 Windshear Detection

Mode 7 provides visual and aural alerts of the proximity of a windshear of sufficient magnitude to be hazardous. Figure 12 shows a block diagram of the windshear logic. The system is capable of detecting severe decreasing performance shears (increasing tailwind/decreasing headwind or downdraft) which present an immediate danger to the aircraft. The system is also capable of detecting severe increasing performance shears (increasing headwind/decreasing tailwind



Bank Angle Warning Envelope, Program Module B01, B02, B03
Figure 10

or updraft). Although an increasing performance shear does not present an immediate danger to the aircraft, it can indicate that the level of atmospheric instability is such that an encounter with a severe decreasing performance shear is likely.

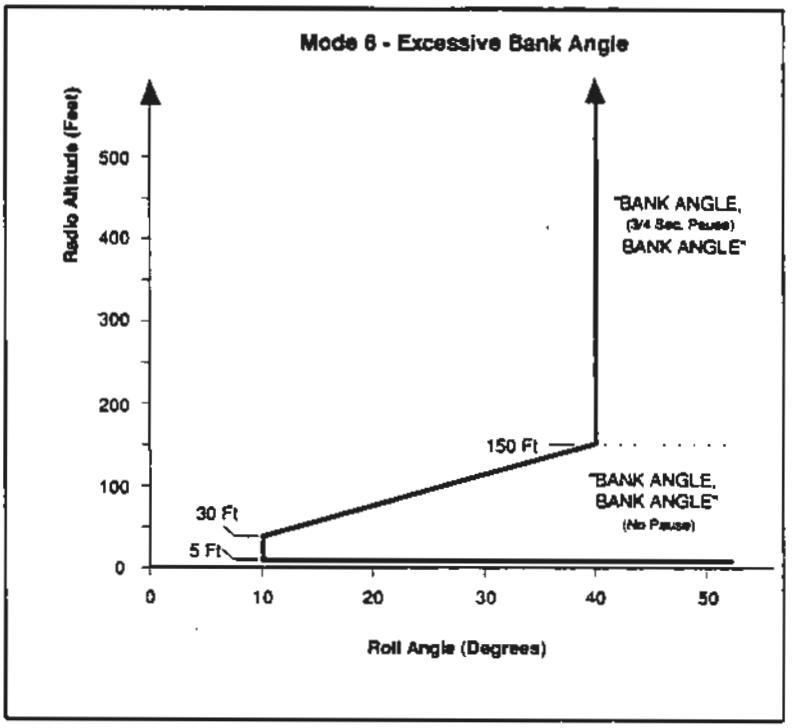
The windshear warning alert is given in the event that the system detects a decreasing performance shear of magnitude greater than the negative warning threshold level. The alert consists of a red warning light in the primary field of view of each pilot, and an aural siren sound followed by the message **WINDSHEAR-WINDSHEAR-WINDSHEAR**. The warning light remains on for as long as the detected windshear condition persists, plus an additional 5 seconds. The aural message is issued once for each detected windshear encounter.

The optional windshear caution alert is given in the event that the system detects an increasing performance shear in excess of the caution threshold level. The windshear caution alert consists of an amber light in the primary field of view of each pilot and if the caution message option has been selected, may be accompanied by the aural message **CAUTION WINDSHEAR**. The optional caution alert is inhibited during a warning alert and for 60 seconds after a warning alert has ceased.

Mode 7 windshear alerting is available under the following conditions:

For takeoff: when airspeed is greater than 90 Kts., body angle of attack (AOA) greater than 4°, and radio height less than 1500 feet and greater than 5 feet. Note that takeoff windshear alerting will remain enabled until the aircraft climbs above 1500 feet or is reconfigured for landing.

On landing approach: when the aircraft is below 1500 feet of radio altitude and above 30 feet of radio height.



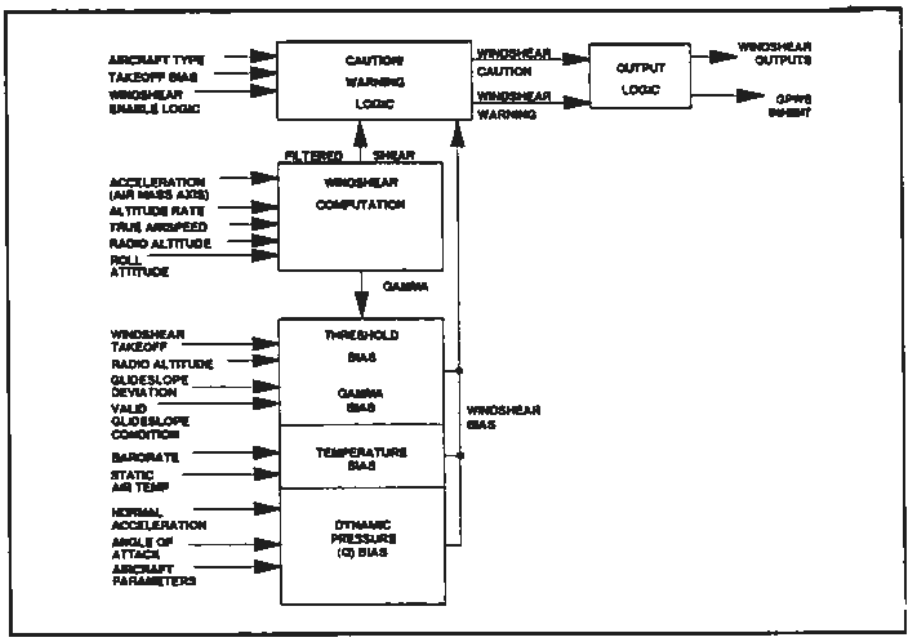
Bank Angle Alert Threshold, Program Module B04 and on
Figure 10.1

Mode 6 Altitude Callouts	
TWENTY FIVE HUNDRED *	
FIFTEEN HUNDRED	FORTY
ONE THOUSAND	THIRTY FIVE
FIVE HUNDRED	THIRTY
FOUR HUNDRED	TWENTY
THREE HUNDRED	TEN
TWO HUNDRED	ONE
ONE HUNDRED	MINIMUMS MINIMUMS
EIGHTY	MINIMUMS
SIXTY	DECISION HEIGHT
FIFTY	

NOTE: Supported with Program Modules B04 and later.

Mode 6 Altitude Callouts
Figure 11

The alert thresholds of Mode 7 are a function of aircraft configuration (takeoff or approach) and are modulated by biases designed to increase the ratio of useful alerts to unwanted alerts. A typical Mode 7 warning envelope is shown in Figure 13.



Mode 7 Block Diagram
Figure 12

In order to reduce the flight deck aural clutter at a time when flight crew intercommunication is vital, the MKVII inhibits aural messages from certain other warning systems while a windshear recovery is in progress. Specifically, when the appropriate logic conditions are satisfied, the basic configuration of the MKVII system causes the aural messages from integrated GPWS functions to be inhibited. At the same time, a traffic alert and collision avoidance system (TCAS) inhibit discrete is output from the system. The GPWS and TCAS aural alerts are inhibited for 5 seconds after the windshear warning message starts, or if the body AOA is greater than 10^{o} and the windshear warning light is on. GPWS visual annunciations will be available at all times.

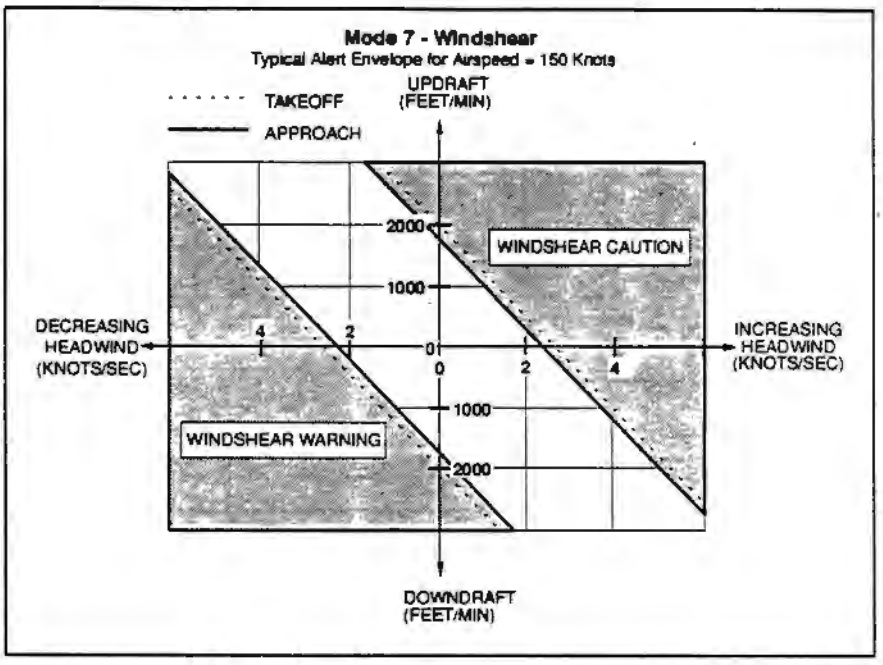
(1) Alert Biases

The filtered shear signal is compared with threshold values to generate the windshear alerts, as described previously. The alert threshold values are modulated by bias signals in order to reduce unwanted alerts to a minimum and to improve the alert time under certain conditions. The biases are called:

a. Gamma bias
b. Q-bias
c. Temperature bias

(a) Gamma Bias

Gamma bias coordinates between the windshear detection and other GPWS functions of the MKVII. The purpose of the gamma bias is to make the program more sensitive which reduces the alert threshold values when the combination of computed flight path angle and glideslope deviation (landing approach mode only) indicates a descent of



Mode 7 Warning Envelope
Figure 13

greater than predetermined value. The gamma bias also increases the alert threshold values when the computed flight path angle indicates that the aircraft is climbing. The purpose of the bias is to provide improved alerts in cases where the windshear is of relatively low magnitude but, because the aircraft is descending at a steeper than usual flight path, a windshear-related hazard exists. Similarly, if the aircraft is climbing steeply, the gamma bias increases alert thresholds, thus reducing the possibility of unwanted alerts.

(b) Q-Bias

The Q-bias function operates when the aircraft is on landing approach and serves to modulate the alert threshold when approach speed exceeds landing speed (VRef). This margin is computed by calculating an approximation to the lift coefficient of the aircraft and comparing this computed value with the value of lift coefficient appropriate for velocity reference (VRef).

If the aircraft is operating at an increased approach speed (increased energy), then the alert thresholds are reduced in sensitivity. Conversely, if the airspeed is lower than VRef, the alert lower thresholds are reduced to sensitize the system for this low energy condition. Thus, when the pilot has anticipated a surface friction windshear and has increased the aircraft approach speed, the algorithm is less prone to unwanted alerts.

(c) Temperature Bias

When ambient air temperature data is available from the aircraft, two forms of alert threshold biasing based on air temperature are provided. Available climb performance of an aircraft is reduced at high ambient air temperatures, and the MKVII windshear

algorithm basic alert thresholds are set for worst case (hot temperature) conditions. In order to reduce the probability of unwanted alerts in conditions of cold ambient temperatures, a bias is added to the threshold values as a non-linear function of static air temperature (SAT), which desensitizes the threshold. A second bias is computed when temperature instability indicates that an encounter with a microburst is probable. This bias is used to decrease the warning threshold value (sensitize the system).

(2) Windshear Options

The windshear caution light and the windshear caution voice can individually be disabled. Therefore, it is possible to have voice alert only, visual alert only, or no alert on positive shear. The windshear caution light is enabled or disabled as part of the aircraft installation wiring. The caution voice is enabled or disabled by the program pins.

H. **Windshear Recovery Guidance**

The MKVII is capable of generating guidance commands for recovery from a windshear encounter. It provides dual-channel pitch and roll windshear recovery guidance and pitch limit indication. Upon receiving a windshear warning, recovery guidance is selected and recovery commands generated by the MKVII are displayed by captain and first officer ADI command bars.

Guidance control laws assist the pilot in managing the available aircraft energy during a windshear encounter. The system uses attitude, vertical speed, radio altitude, and stick shaker margin information to adjust pitch attitude so that the distribution of energy between potential energy and kinetic energy reflects the immediate requirements.

If the aircraft is very close to the terrain, the system will emphasize potential energy and sacrifice kinetic energy by increasing pitch. If there is adequate terrain clearance, the emphasis is placed on kinetic energy by reducing the pitch. The pitch command computation avoids stall, but short duration excursions of AOA beyond the value required to activate the stall warning system may occur, especially in turbulent conditions.

I. **Mark II Emulation Mode**

MKVII systems with B03 and higher versions of the program module provide a configuration that emulates Mark II warning computer operation. This configuration allows the MKVII to directly replace an existing Mark II warning computer with no aircraft wiring changes and with minimal operational impact.

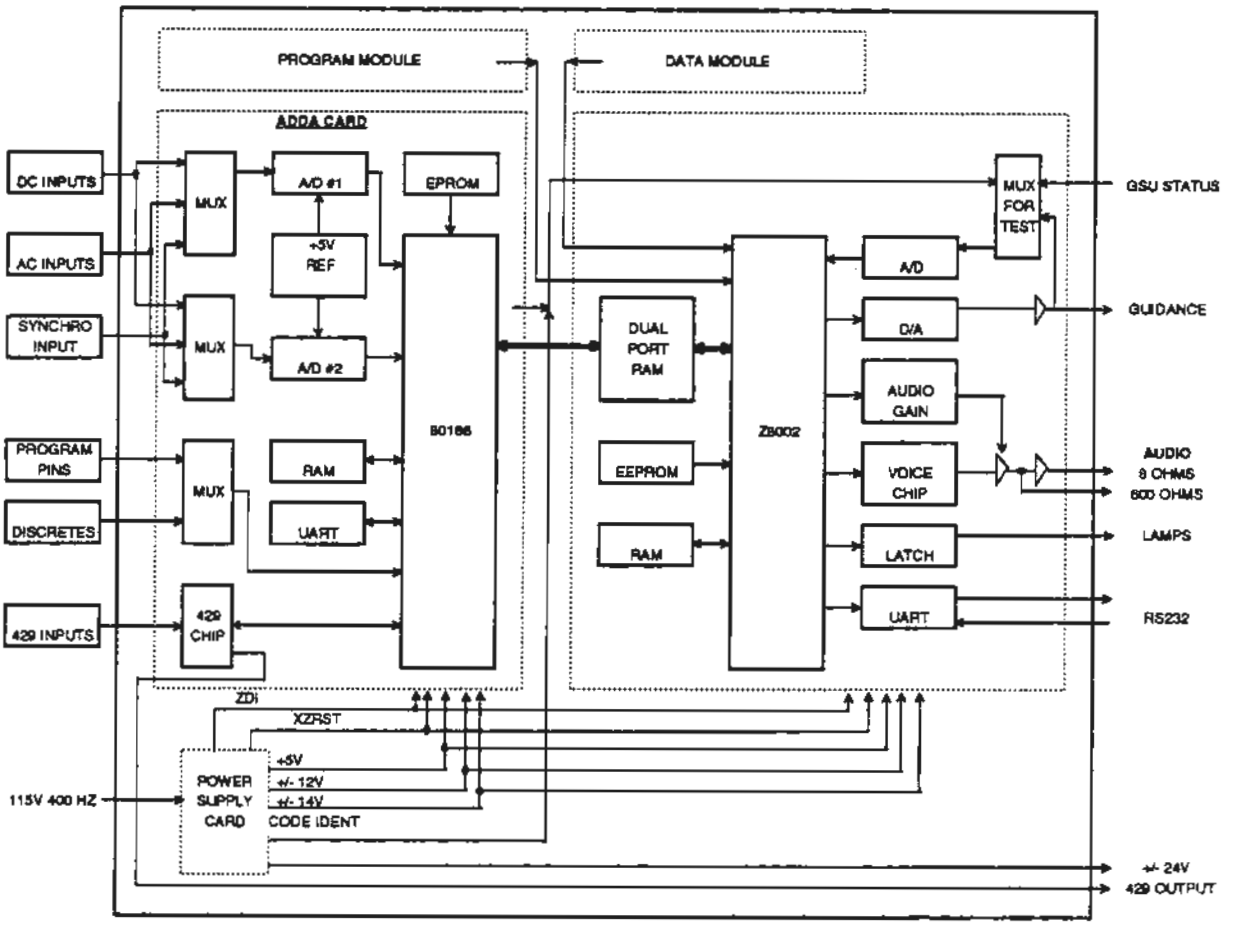
J. **Mode Switching**

To provide appropriate GPWS and windshear warnings, the MKVII continuously monitors the operational status of the aircraft to determine the current phase of flight. The MKVII uses several variables such as radio altitude, airspeed, gear position, flap position, and time of flight to determine if the aircraft is operating in the takeoff or cruise/approach phase of flight and whether the aircraft is on the ground or in the air. Different takeoff/approach logic is used for the GPWS and windshear functions. These modes are mutually exclusive in nature and therefore always reside in one of two possible states. The status of these modes are stored in nonvolatile memory to avoid inadvertent selection of an improper mode during power loss.

13. **Theory of Operation**

The theory of operation for the MKVII is divided into subassembly groups and focuses on the hardware with a description of how the hardware and software interface. If a more detailed description of an individual active device is needed, data sheets for the active devices are included with the subassembly schematics in TESTING AND TROUBLESHOOTING.

Figure 14 shows a block diagram of the MKVII subassemblies and the address, data, and power



MKVII Hardware Block Diagram
Figure 14

bus.

A. **Program/Data Modules**

The program module includes PVM microprocessor boot code and operational software and constant interface through PVM J11. It is selected by the signal ZPG-MOD from the PVM Extended Memory Decoder (U38) (EMD). The data module contains non-executable data and scaling parameters for various aircraft types. The data module interfaces with the PVM microprocessor through PVM J10 and is selected by ZDATMOD from the EMD.

Both modules are accessed by the PVM through the 16-bit mux address/data bus. The PVM has an interlock circuit designed to remove power to the modules and reset the PVM microprocessor using the signal ZRESET if one or the other module is removed. The interlock circuit is designed to prevent the microprocessor from trying to operate with a module missing.

ZPGMODIN and ZDATMODIN signals are tied to +5Vdc through pullup resistors on the PVM. When the modules are installed they provide ground to pin 1 on PVM J10 and J11. +5Vdc is

dropped across the pullup resistors. The resulting logic low signals for ZPGMODIN and ZDATMODIN are ANDed in the PVM gate array (U19) using Demorgan's Theorem. The gate array outputs ZMODPWR to turn on Q7 which in turn allows +5V to the modules. A high logic level on ZPGMODIN or ZDATMODIN causes the gate array to issue ZRESET to the microprocessors and set ZMODPWR high, removing +5Vdc from the module that is still installed in the unit.

B. Signal Inputs and Outputs

The MKVII inputs and outputs address three main areas of process: ground proximity, windshear, and recovery guidance. Figure 15 shows an interface block diagram of ADDA and PVM, the inputs and outputs, where the assemblies interface, and what inputs and outputs are related to in the three areas of process. Inputs and outputs from J1 communicate with the aircraft through the backplane assembly. J2 inputs and outputs communicate directly with the aircraft sensors and controls.

C. ADDA Board

The ADDA uses an 80C186 microprocessor to interface hardware and software. In the following paragraphs, the operation of the microprocessor and the signal processing operations are given. If more detailed information is required for troubleshooting the 80C186 processor, see the Intel 80C186 microprocessor technical manual. Figure 16 shows a functional block diagram of the ADDA.

(1) 80C186 Microprocessor Operation

The 80C186 registers are set as follows:

```
UMCS = E038(H):  System memory, 64K (CFFFFH - FFFFFH)
MPCS = 82B8(H):  Mid-range memory select, 16K (each mid-range is 4K)
PACS = 0438(H):  Peripheral Chip select base address, (04000H)
LMCS = 03F8(H):  Vector interrupt table, 16K (00000H - 04000H)
MMCS = 09F8(H):  Specifies base address of mid-range memory
                 select (08000H)
```

(2) ADDA Board Memory Map

Figure 17 shows the Memory Map for the ADDA board.

(3) I/O Address Map

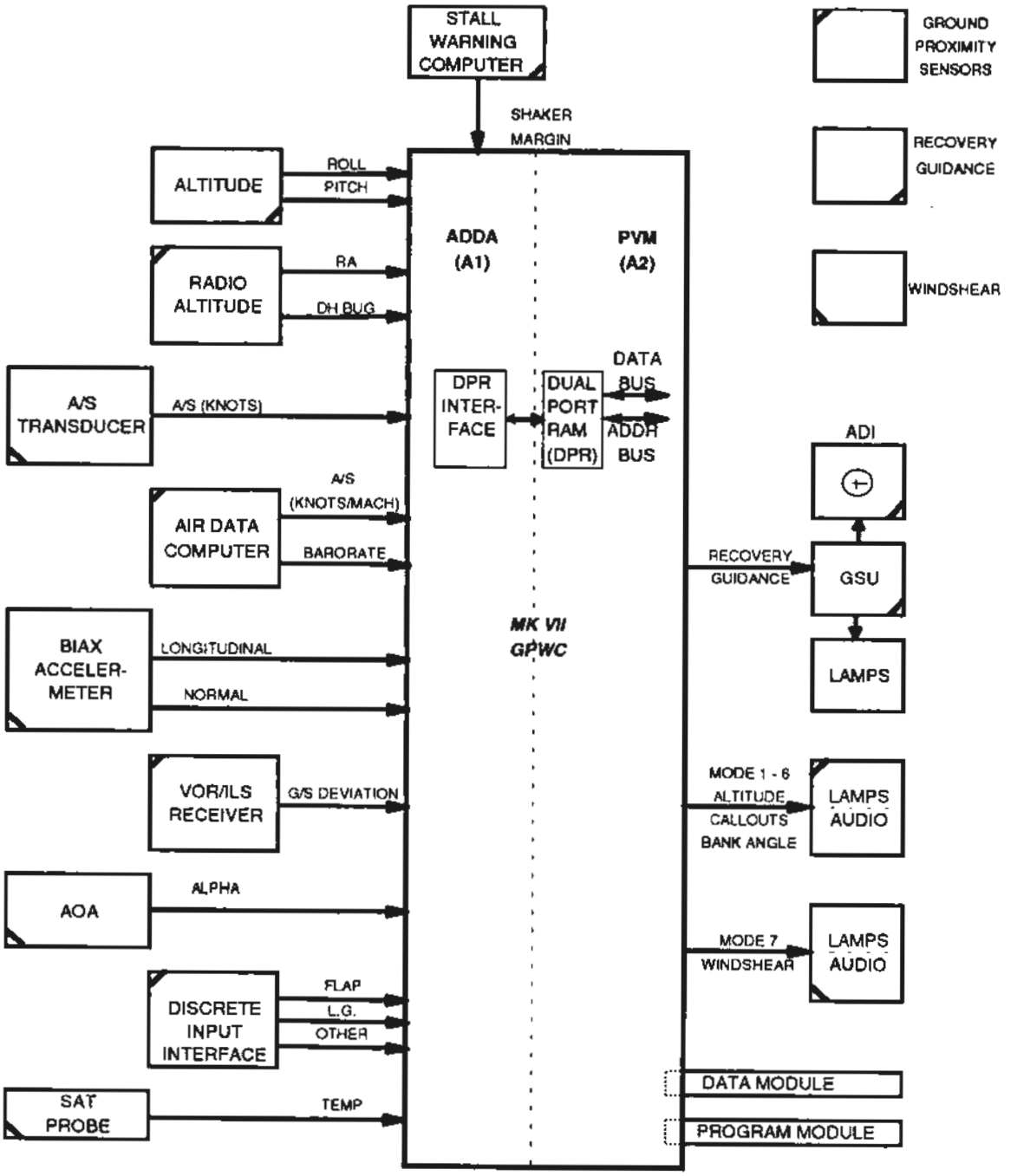
Figure 18 shows the I/O Address Map for the ADDA board.

(4) Discrete Inputs

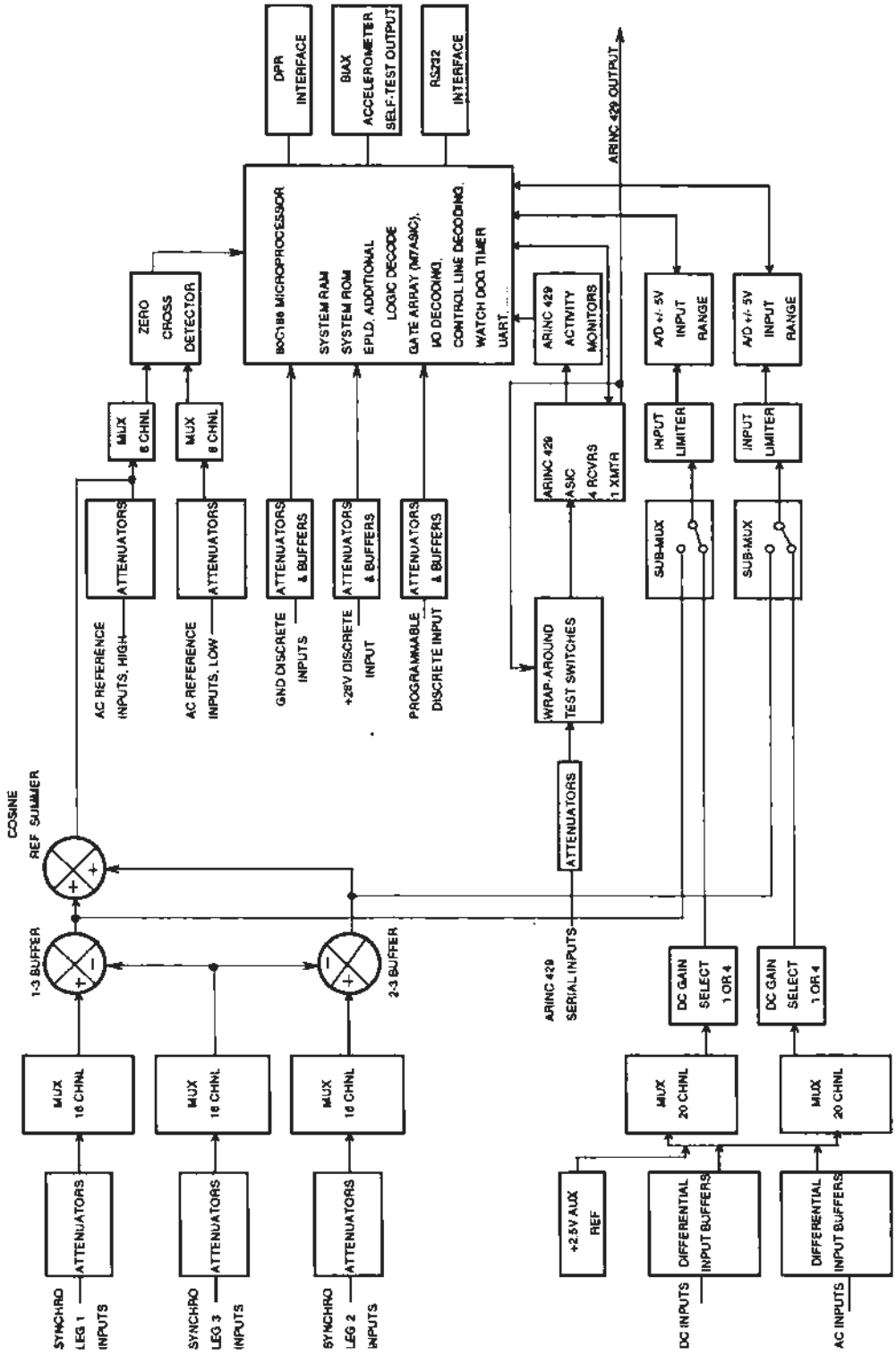
The data registers for the discrete inputs are listed in the following:

```
ZDISC1 – Discrete input port #1.  Refer to Figure 19.
Address:  4000H
Access mode:  I/O word, read only


ZDISC2 – Discrete Input Port #2.  Refer to Figure 20.
Address:  4080H
Access mode:  I/O word, read only
```



MKVII ADDA, PVM Signal Block Diagram
Figure 15



ADDA Functions Block Diagram
Figure 16

Address Range	Description
00000-03FFF	System RAM (byte or word addressable)
04000-07FFF	Reserved for future System RAM
08000-08FFF	Dual Port RAM (word addressable only)
09000-09FFF	A/D Hold Command
0A000-0AFFF	A/D #1 Data/Status Registers
0B000-0BFFF	A/D #2 Data/Status Registers
0C000-0FFFF	Not Used
E0000-EFFFF	Future System ROM
F0000-FFFFF	System ROM

ADDA Board Memory
Figure 17

ADDRESS	NAME	DESCRIPTION
4000	ZDISC1	Discrete Input Port #1
4080	ZDISC2	Discrete Input Port #2
4100	ZDISC3	Discrete Input Port #3
4180	V429CS0	429 RCVR 0 Status/Control
4182	V429DL0	429 RCVR 0 Data/Label
4184	V429CS1	429 RCVR 1 Status/Control
4186	V429DL1	429 RCVR 1 Data/Label
4188	V429CS2	429 RCVR 2 Status/Control
418A	V429DL2	429 RCVR 2 Data/Label
418C	V429CS3	429 RCVR 3 Status/Control
418E	V429DL3	429 RCVR 3 Data/Label
419D	X429CONT	429 XMTR Control
4192	X429DATA	429 XMTR Data
4194		429 RCVR Data MUX
4196		429 Clock MUX Test
4198	V429MS	429 Main Status
4200	LATSL2	Dutput Data Latch #2
5022	DOGRST	Watch Dog Timer Reset Port
50C2		Interrupt Controller Status
50E2		UART Data Register
5100	LATSL1	Output Data Latch #1
5142	V429RESET	VLSI 429 Activity Latch Reset
5180	ZPPIN1	Program Pin Input Port #1
51CD	ZPPIN2	Program Pin Input Port #2

ADDA I/O Address Map
Figure 18

ZDISC3 – Discrete Input Port #3. Refer to Figure 21.
Address: 4100H
Access mode: I/O word, read only

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	J1A-25	<Decision height	>Decision height
1	J1A-01	Low volume	Normal volume
2	J1B-34	Cancel Mode 5	Normal
3	J2-K12	T.O. Thrust #1	Not T.O. Thrust #1
4	J2-G4	Select Menu B	Select Menu A
5	J1B-23	Landing gear down	Landing gear up
6	J1B-24	Not landing flap	Landing flap #1
7	J2-J11	Stall #1 valid	Stall #1 invalid
8	J1A-03	Enable Mode 5	Normal
9	J1A-05	Inhibit Mode 5	Normal
10	J1B-16	Audio suppress	Normal
11	J1B-22	Self test	Normal
12	J2-D5	T.O. Thrust #2	Not T.O. Thrush #2
13	J2-E14	Guidance deselect	Not Guidance deselect
14	J2-C4	Stall #2 valid	Stall #2 invalid
15	REFINT	Negative reference	Posltive reference

Discrete Input Port #1
Figure 19

Bit	Pin Mnemonlc	Bit=0 description	Bit=1 description
0	J1B-07	Landing gear up	Landlng gear down
1	J1A-24	Landing flap #1	Not landing flap #1
2	J2-G3	Accel #1 invalid	Accel #1 valid
3	J1B-01	Normal	Enable Mode 5
4	J1B-02	Normal	Inhibit Mode 5
5	J1B-27	B/R #1 invalid	B/R #1 valid
6	J2-K11	Attitude #1 invalid	Attitude #1 valid
7	J1B-26	Glide Slope invalid	G/S valid
8	J2-E15	Not Stick Shaker	Stick Shaker
9	J2-G5	Speed invalid	Speed valid
10	J1B-19	R/A invalid	R/A valid
11	J2-D4	Attitude #2 invalid	Attitude #2 valid
12	J1B-08	Normal	Audio suppress
13	J2-D11	Accel #2 invalid	Accel #2 valid
14	J2-D12	B/R #2 invalid	B/R #2 valid
15	DOGSTS	Power-up Reset	Watchdog time-out

Discrete Input Port #2
Figure 20

Bits 0 to 3 are used in conjunction with V429RESET to detect 429 activity on the 429 bus. Writing to V429RESET sets these bits to 0. Activity on the bus latches the bit to 1, indicating

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	Bus #1	No activity	Activity
1	Bus #2	No activity	Activity
2	Bus #3	No activity	Activity
3	Bus #4	No activity	Activity
4	J2-E13	Ground A/P discon	+28V A/P disc
5	J2-C5	Ground TOGA #2	+28V TOGA #2
6	J2-E12	Ground spare #3 disc	+28V spare #3 disc
7	WRMSRT	Power up >1 sec	Power up <1 sec
8	J2-J12	Ground TOGA #1	+28V TOGA #1
9	J2-G2	Ground spare #2 disc	+28V spare #2 disc
10	J2-G1	Ground spare #1 disc	+28V spare #1 disc
11		No A/D calibration	A/D calibration
12	ZEOC1	A/D #1 complete	A/D #1 converting
13	ZEOC2	A/D #2 complete	A/D #2 converting
14	ZEDT1	A/D #1 tracking	A/D #1 acquiring
15	ZEOT2	A/D #2 tracking	A/D #2 acquiring

Discrete Input Port #3
Figure 21

receiving activity on the bus.

(5) ARINC 429 Transceiver

The ARINC 429 transceiver interface control and status registers give an overview of the ARINC 429 transceiver.

V429CS0 – VSLI 429 RCVR 0 control/status register.

NOTE: *To properly interpret the following list, it is necessary to know if the register is in the write or read mode at the time the status is checked. Figure 22 shows the read mode and Figure 23 shows the write mode.*

```
Address:  4180
Access mode:  I/O byte, write/read

V429CS1 – VSLI 429 RCVR 1 Control/status register.
Bit definitions are the same as V429CS0.
Address:  4184
Access mode:  I/O byte, write/read

V429CS2 – VSLI 429 RCVR 2 Control/status register.
Bit definitions are the same as V429CS0.
Address:  4188
Access mode:  I/O byte, write/read

V429CS3 – VSLI 429 RCVR 3 Control/status register.
Bit definitions are the same as V429CS0.
```

Read Mode (Status)			
Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	D0	Low speed (12.5 KHZ)	High speed (100 KHZ)
1	D1	Receiver disabled	Receiver enabled
2	D2	Auto parity enabled	Auto parity disabled
3	D3	Frame size is 32 bits	Frame size is 24 bits
4	D4	Label recognition enabled	Label recognition disabled
5	D5	No frame overrun error	Frame overrun error
6	D6	No parity error	Parity error
7	D7	Not read label mode	Read label mode

ARINC 429 Transceiver Read Mode
Figure 22

Write Mode (Control)			
Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	D0	Low speed (12.5 KHZ)	High speed (100 KHZ)
1	D1	Disabled receiver	Receiver enabled
2	D2	Enable auto parity	Auto parity disabled
3	D3	Set frame size = 32 bits	Frame size is 24 bits
4	D4	Enable label recognition	Label recognition disabled
5	D5	Enable label RAM write	Disable label RAM write
6	D6	Do not clear status flags	Clear status flags
7	D7	Do not clear label RAM	Clear label RAM

ARINC 429 Transceiver Write Mode
Figure 23

Address: 418C

Access mode: I/O byte, write/read
V429DL0 – VSLI429 RCVR 0 data/label register.

This register is used to read ARINC 429 data packets (32 bits) that are received on channel 0, or to program channel 0 to recognize only those data packets with specific labels. A data packet is read by reading V429DLO four times consecutively. The channel is programmed to recognize labels by writing the label (with bits reversed) to register V429DLO.

Address: 4182
Access mode: I/O byte, write/read

V429DL1 – VSLI429RCVR 1 Data/label register. The function is the same as

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	D0	Frame not ready	Frame ready on channel 0
1	D1	Frame not ready	Frame ready on channel 1
2	D2	Frame not ready	Frame ready on channel 2
3	D3	Frame not ready	Frame ready on channel 3
4	D4	Low speed (12.5 KHZ)	High speed (100 KHZ)
5	D5	Transmitter not empty	Transmitter empty
6	D6	Transmitter not enabled	Transmitter enabled
7	D7	Chip is not ready	Chip is ready

429 Main Status Register
Figure 24

V429DL0 except that it is used with channel 1.

Address: 4186
Access mode: I/O byte, write/read

V429DL2 – VSLI429RCVR 1 Data/label register.
The function is the same as V429DL0 except that it is used with channel 2.

Address: 418A
Access mode: I/O byte, write/read

V429DL3 – VSLI429RCVR 1 Data/label register.
The function is the same as V429DL0 except that it is used with channel 3.

Address: 418E
Access mode: I/O byte, write/read

V429MS – VLSI429 Main Status Register
Refer to Figure 24.

Address: 4198
Access mode: I/O byte, read only

V429CONT – VLSI429 Transmitter Control Register
Refer to Figure 25.

Address: 41908
Access mode: I/O byte, write only

X429DATA – VLSI ARINC 429 Transmitter Data Register.

This register is used to transmit a 32-bit ARINC 429 data packet. A packet is transmitted by writing the four bytes of data to this register consecutively. The label (with bits reversed) must be the first byte written.

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	D0	Select low speed	Select high speed
1	D1	Disable Transmitter	Enable Transmitter
2-7	02-7	(Not used)	(Not used)

ARINC 429 Transmitter Control Register
Figure 25

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	D0	(Not used)	(Not used)
1	D1	(Not used)	(Not used)
2	D2	Disable xmtr parity	Enable xmtr parity
3	D3	Disable loop back	Enable loop back
4-7	D4-7	(must be zero)	

ARINC 429 Transmitter Auxiliary Control Register
Figure 26

Address: 4192
Access mode: I/O byte, write only

V429AUX – VLSI ARINC 429 Transmitter Auxiliary Control Register
Refer to Figure 26.

Address: 419C
Access mode: I/O byte, write only

Register

(6) Output Data Latch #2

LATSL2 – Data Output Latch #2. Refer to Figure 27. Address: 4200H Access mode: I/O word, write only

(7) Output Data Latch #1

LATSL1 – Data Output Latch #1. Refer to Figure 28.

Address: 5100H
Access mode: I/O word, write only
Bits 0 - 4: 2-wire mux address
Bits 8 - 11: 3-wire mux address
Bits 12 - 14: Reference input mux address

Figure 29 shows the relationship between 2-wire devices, their input address, and the ADC

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	1Z5PG1	A/D #1 gain of 5	A/D #1 gain of 1
1	1Z5PG2	A/D #2 gain of 5	A/D #2 gain of 1
2	UZBSP1	Bipolar spare 1&2	Unipolar spare 1&2
3	UZBSP2	Bipolar stall 1&2	Unipolar stall 1&2
4	PP4-Z+	Ground A/P discon	+28V A/P discon
5	PP5-Z+	Ground TOGA sel #2	+28V TOGA sel #2
6	PP6-Z+	Ground Spare disc #3	+28V Spare disk #3
7	J15-13	Guidance #2 invalid	Guidance #2 valid
8	PP1-Z+	Ground TOGA sel #1	+28V TOGA sel #1
9	PP2-Z+	Ground Spare disc #1	+28V Spare disc #1
10	PP3-Z+	Ground Spare disc #2	+28V Spare disc #2
11	429TST	429 wrap-around	Normal input
12	ACSTLO	See table below	
13	ACSTHI	See table below	

ACSTHI	ACSTLO	Function
0	0	Zero accelerometer self test output
0	1	Negative accelerometer self test output
1	0	Positive accelerometer self test output
1	1	Do not use

Output Data Latch #2
Figure 27

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
5	3Z2SEL	2 wire inputs	3 wire inputs
6	AOASEL	DC AOA inputs	AC AOA inputs
7	J17-5	Guidance #1 inval	Guidance #1 valid
15	2Z3SYN	Normal synchros	2 wire synchros

Output Data Latch #1
Figure 28

that converts their signals.

Figure 30 shows the relationship between 3-wire devices, their input address, and the ADC that converts their signals.

Following is a list of the addresses of reference inputs:

Address	A/D #1	A/D #2
0	Radio Altitude	Radio Altitude Validity
1	Glideslope Deviation	Glideslope Oev. Validity
2	Barometric Altitude Rate #1	Barometric Altitude Rate #2
3	Mach	PVM Reference (2.5V)
4	Static Air Temperature	Static Air Temperature Reference
5	Angle of Attack #1	Angle of Attack #2
6	Normal Acceleration #1	Normal Acceleration #2
7	Longitudinal Accel #1	Longitudinal Acceleration #2
8	Spare Input #1	Spare Input #2
9	Stall Margin #1	Stall Margin #2
A	Flap Position #1	Flap Position #2
B	(Internal Spare #1)	(Internal Spare #2)
C	AC Baro Alt Rate Ref #2	AC Baro Alt Rate Signal #2
D	0.0000V Offset Reference	0.0000V Offset Reference
E	2.5V Auxiliary Reference	2.5V Auxiliary Reference
F	4.8387V Gain Reference	4.8387V Gain Reference
10	AC Baro Alt Rate Signal #1	AC Baro Alt Rate Reference #1
11	AC Barometric Altitude	AC Baro Alt Rate Reference #1
12	AC Static Air Temperature	AC Static Air Temperature Ref
13	(Internal Spare #3)	(Internal Spare #4)
18	A/D Reset	A/D Reset

2-Wire Devices Input Address
Figure 29

0 – Internal cosine reference of selected synchro in the data latch #2 by address 3A0-3A3.
1 – Barometric altitude rate #1
2 – Static air temperature
3 – Barometric altitude rate #2
4 – Spare #1
5 – Spare #2
6 – Unused internal spare
7 – Unused internal spare

(8) Watch Dog Timer

The watchdog timer is used to ensure the software is operating properly. The watchdog timer is part of the gate array IC (U53). It has a reset port (DOGRST, internal to the gate array) and an output line (ZRES). At power-up the output line goes high. The output line remains high until there is a time-out. A time-out occurs if the timer is not reset at least once every 131 milliseconds. If a time-out occurs, the output line goes low for 131 milliseconds and then goes high again. This resets the ADDA microprocessor. If DOGSTS from the gate array is 1, a watchdog timeout is read by the microprocessor when ZDISC2 is set.

DOGRST – Watchdog reset port.
Address: 5022
Access mode: I/O word, write only

Address	A/D #1	A/D #2
0	Mach or CAS 1-3 (X-Z)	Mach or CAS 2-3 (Y-Z)
1	Flap Pos #1 1-3 (X-Z)	Flap Pos #1 2-3 (Y-Z)
2	Pitch #1 Att 1-3 (X-Z)	Pitch #1 Att 2-3 (Y-Z)
3	Roll #1 Att 1-3 (X-Z)	Roll #1 Att 2-3 (Y-Z)
4	AOA #1 1-3 (X-Z)	AOA #1 2-3 (Y-Z)
5	Stall Margin #1 1-3 (X-Z)	Stall Margin #1 2-3 (Y-Z)
6	Spare #1 1-3 (X-Z)	Spare #1 2-3 (Y-Z)
7	(Unused internal spare)	(Unused internal spare)
8	Baro Alt Fine 1-3 (X-Z)	Baro Alt Fine 2-3 (Y-Z)
9	Flap Pos #2 1-3 (Y-Z)	Flap Pos #2 2-3 (X-Z)
A	Pitch #2 Att 1-3 (Y-Z)	Pitch #2 Att 2-3 (X-Z)
B	Roll #2 Att 1-3 (Y-Z)	Roll #2 Att 2-3 (X-Z)
C	AOA #2 1-3 (Y-Z)	AOA #2 2-3 (X-Z)
D	Stall Margin #2 1-3 (Y-Z)	Stall Margin #2 2-3 (X-Z)
E	Spare #2 1-3 (Y-Z)	Spare #2 2-3 (X-Z)
F	(Unused internal spare)	(Unused internal spare)

3-Wire Devices Input Address
Figure 30

(9) Gate Array Interrupt Controller

The ADDA gate array includes an interrupt controller that can receive six channels of interrupts. Two of the interrupts are internally generated from the gate array RS232 receive and transmit functions. The four external interrupt channels are connected to the four ARINC 429 bus interrupts. These interrupts all cascade into the 80186's interrupt 0. The gate array interrupt sources are mapped according to the following list:

```
Interrupt 0:  ARINC 429 label hit on bus 3
Interrupt 1:  RS232 data received
Interrupt 2:  RS232 transmitter ready
Interrupt 3:  ARINC 429 label hit on bus 0
Interrupt 4:  ARINC 429 label hit on bus 1
Interrupt 5:  ARINC 429 label hit on bus 2
```

A complete description of the bit functions of each register is included in TESTING AND TROUBLESHOOTING. Figure 31 shows a summary of the register definitions.

```
ZIMREG – Interrupt Controller Mask Register
Address:  50A2
Access Mode:  I/O byte, write only
```

(10) VLSI 429 Activity Latch Reset

```
V429RESET – VLSI 429 Activity Latch Reset
Address:  5142H
Access mode:  I/O word, write only
```

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	IMASK0	Disable interrupt 0	Enable interrupt 0
1	IMASK1	Disable interrupt 1	Enable interrupt 1
2	IMASK2	Disable interrupt 2	Enable interrupt 2
3	IMASK3	Disable interrupt 3	Enable interrupt 3
4	IMASK4	Disable interrupt 4	Enable interrupt 4
5	IMASK5	Oisable interrupt 5	Enable interrupt 5
6	(none)	(not used)	(not used)
7	INTENBL	Disable all (override)	Allow interrupts to be enabled

Register Definitions
Figure 31

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	J2-F1	A/C select #1	Not A/C select #1
1	J2-F2	A/C select #2	Not A/C select #2
2	J2-F3	A/C select #3	Not A/C select #3
3	J2-F4	A/C select #4	Not A/C select #4
4	J2-F5	A/C select #5	Not A/C select #5
5	J2-F6	A/C select #6	Not A/C select #6
6	J2-F7	A/C select #7	Not A/C select #7
7	J2-F8	A/C select #8	Not A/C select #8
8	J2-F9	A/C select #9	Not A/C select #9
9	J2-F10	A/C select #10	Not A/C select #10
10	J2-F11	A/C select #11	Not A/C select #11
11	J1A-14	Reverse flap logic	Normal flap logic
12	J1A-29	Warn select #1	Not warn select #1
13	J1A-28	Warn select #2	Not warn select #2
14	J2-G8	Enable windshear	Inhibit windshear
15	J1A-32	Alt R/A scale	Normal R/A scale

Program Pin Input Port #1
Figure 32

A write to V429RESET resets the bits 0 through 3 of ZDISC3 (discrete input port #3) to zero.

(11) Program Pin Inputs

ZPPIN1 is the Program Pin input port #1. Figure 32 shows the bit to pin relationship.

ZPPIN2 is the Program Pin input port #2. Figure 33 shows the bit to pin relationship.

Bit	Pin Mnemonic	Bit=0 description	Bit=1 description
0	J2-F12	Call vocab #1	Not call vocab #1
1	J2-F13	Call vocab #2	Not call vocab #2
2	J2-F14	Call vocab #3	Not call vocab #3
3	J2-F15	Call vocab #4	Not call vocab #4
4	J1A-27	Reduce audio	Normal audio
5	J2-G13	Spare #1 active	Spare #1 inactive
6	J2-G14	Spare #2 active	Spare #2 inactive
7	J2-G15	Spare #3 active	Spare #3 inactive
8	J2-G12	Enable envelope	Inhibit envelope
9	J2-G11	QFE baro altitude	Radio altitude
10	J2-G9	Volume select #1	Not volume select #1
11	J2-G10	Volume select #2	Not volume select #2

Bits 12-15 not used

Program Pin Input Port #2
Figure 33

(12) Data Acquisition for the ADDA

The ADDA board acquires input signals from the aircraft sensors and converts the data to signals the PVM can use to determine warning status. In order to describe the ADDA operation, one input signal from each of the seven types of inputs is traced through its processes on the ADDA. All signals from the same type can be presumed to function exactly as other signals from that type.

Radio altitude is the most common input signal to the WC for all the alert/warning modes and is discussed in the following paragraphs. This signal represents the vertical distance between the aircraft and the ground. The radio altimeter system is designed to read exactly zero feet altitude just as the landing gear first touches the runway. The signal scaling is linear at +0.020Vdc/feet (0.0Vdc) to +480 feet (+10.00Vdc) and then becomes non-linear as the signal increases to +27.299Vdc at 2800 feet. A special algorithm is used to linearize the logarithmic portion of the signal while maintaining an accurate slope value for radio altitude rate computation.

Radio altitude data is sampled every 4.096 milliseconds and summed until 8 samples are collected in the required 32.768 milliseconds. The total from the 8 samples is then averaged and scaled at 1.0 foot per 16 least significant bits (LSB) for further processing. The averaging of the samples provides better altitude rate accuracy for the time when the input data is changing.

Following is a list of the signal types and the names of signals processed in the same manner as radio altitude:

(a) DC Analog Input Signals

```
Radio Altitude:  ARINC 552A
Radio Altitude:  ALT 50/55
OC Barometric Altitude Rate #1:  ARINC 595
```

DC Barometric Altitude Rate #2: ARINC 595
Glideslope Deviation Low Level: ARINC 547 or 551
Glideslope Deviation High Level: ARINC 578
DC Airspeed: ARINC 575
DC Airspeed: Special
Static Air Temperature (SAT): ARINC 565
Normal Acceleration #1: SDC Biaxial Accelerometer
Normal Acceleration #2: SDC Biaxial Accelerometer
Longitudinal Acceleration #1: SDC Biaxial Accelerometer
Longitudinal Acceleration #2: SDC Biaxial Accelerometer
Captains' Guidance Switching Unit (GSU) Validity
First Officers' GSU Validity
AOA Potentiometer #1
AOA Potentiometer #2
Flap Position #1
Flap Position #2
Stall Margin #1
Stall Margin #2
Spare Input #1
Spare Input #2

(b) AC Analog Input Signals (400 Hz nominal)

AC Barometric Altitude Rate #1: ARINC 545A, 565
AC Barometric Altitude Rate #2: ARINC 545, 565
AC Barometric Altitude - Coarse: ARINC 545A, 565
Static Air Temperature (SAT): SAT Indicator
Spare AC Reference #1
Spare AC Reference #2

(c) Synchro Input Signals (400 Hz nominal)

CAS Synchro: ARINC 545A, 565
Barometric Altitude Fine Synchro: ARINC 545A, 565
Roll Attitude #1: ARINC 561
Roll Attitude #2: ARINC 561
Pitch Attitude #1 Synchro: ARINC 561
Pitch Attitude #2 Synchro: ARINC 561
AOA Synchro #1
AOA Synchro #2
Flap Position Synchro #1
Flap Position Synchro #2
Stall Margin Synchro #1
Stall Margin Synchro #2
Spare Synchro #1
Spare Synchro #2

(d) Discrete Input Signals

Barometric Altitude Rate #1 Validity: +28Vdc
Barometric Altitude Rate #2 Validity: +28Vdc
Radio Altimeter Validity - Special
Glideslope Validity - Special

Airspeed Validity: +28Vdc
Attitude Validity #1: +28Vdc
Attitude Validity #2: +28Vdc
Stall Warning Stick Shaker +28Vdc
Accelerometer #1 Validity #1: +28Vdc
Accelerometer #2 Validity #1: +28Vdc
Flap Range #1A: +28Vdc
Flap Range #1B: +28Vdc
Flap Range #2A: +28Vdc
Flap Range #2B: +28Vdc
Slat Position #1A: +28Vdc
Slat Position #1B: +28Vdc
Slat Position #2A: +28Vdc
Slat Position #2B: +28Vdc
Accelerometer Self Test: + 28Vdc

(e) Ground Seeking Discrete Inputs

Radio Altitude Decision Height: Ground
Mode 6 and Altitude Callout Volume Control: Ground
Glideslope Mode Manual Inhibit (Cancel): Ground
Self Test Initiation: Ground
Altitude Callouts Menu A/B Select: Ground
Stall Margin Validity #1: Ground
Stall Margin Validity #2: Ground
Guidance De-select: Ground
Takeoff Thrust #1: Ground
Takeoff Thrust #2: Ground
Stall Warning Stick Shaker #1: Ground
Stall Warning Stick Shaker #2: Ground

(f) Combination +28Vdc and Ground Seeking Discrete Inputs

Landing Gear Position
Landing Flap Position
Glideslope Mode Enable or ILS Frequency Selected
Glideslope Mode Inhibit or ILS Backcourse In Progress
Audio Output Suppress Activation
TOGA #1
TOGA #2
Autopilot Disconnect
Spare #1
Spare #2
Spare #3

(g) Program Pin Input Signals

Flap Discrete Reversal Select
Warning Envelope Select #1
Warning Envelope Select #2
Windshear Alert/Warning Select
Audio Reduction Select
Audio Volume Select #1

```
Audio Volume Select #2
Envelope Modulation (Airport Recognition) Select
Radio/QFE Barometric Altitude Callout Select
Altitude Callout Vocabulary Select #1
Altitude Callout Vocabulary Select #2
Altitude Callout Vocabulary Select #3
Altitude Callout Vocabulary Select #4
Aircraft/Interface/Warning Threshold Select #1
Aircraft/Interface/Warning Threshold Select #2
Aircraft/Interface/Warning Threshold Select #3
Aircraft/Interface/Warning Threshold Select #4
Aircraft/Interface/Warning Threshold Select #5
Aircraft/Interface/Warning Threshold Select #6
Aircraft/Interface/Warning Threshold Select #7
Aircraft/Interface/Warning Threshold Select #8
Aircraft/Interface/Warning Threshold Select #9
Aircraft/Interface/Warning Threshold Select #10
Aircraft/Interface/Warning Threshold Select #11
Alternate Radio Altimeter Scale Factor Select
Windshear Guidance Select
Spare Select #1
Spare Select #2
```

(13) ADDA DC Input Signal Acquisition

The MKVII DC inputs of radio altitude are standardized to ARINC 552A criteria. The input connections for the DC radio altimeter are shown in the following list:

MKVII	INTERNAL	ADDA(S2)	AR3A(S4)
+ J1B - 20	J4 - 7	J11 - 7	Pin 2
- J1B - 21	J4 - 6	J11 - 6	Pin 3

The input from the radio altimeter (RA) DC sensor is taken from the MKVII rear panel connector to operational amplifier AR3A. Amplifier AR3A has a gain of 0.243. Pull up resistors R53 (+12Vdc) and R54 (-12Vdc) bias AR3A into saturation if the input signal is lost. Voltage reference is a +5Vdc bias voltage that allows for a constant operational amplifier output of ±5Vdc with a -1 to +28Vdc input. Normal input is ±5Vdc. This reference is always used with RA. Optional biasing of this signal is programmable using ADDA microprocessor signals UZBSP1 and UZBSP2. The output of AR3A is inverted by buffer AR3B and sent to AC/DC input mux (U2).

RA validity MKVII rear panel input is J1B pin 19 and goes to ADDA J10 pin-12 to AR15C. It can be +28Vdc or low level validity of +3.5 to 4.5Vdc. AR15C has a gain of 1.

The AR15C output is inverted. VR301 is a 4.7Vdc zener used to prevent 28Vdc validity from saturating AR15C which would cause the input limiter circuit to turn on and clamp RA validity signal. The output of AR15C goes to AC/DC input mux U6. RAVAL and RADALT signals also control the output of U2 (1A) and U6 (1B) and switch the output of both to the DC gain select circuit.

Signals From the Microprocessor

	ZHOLD	ZAD2CS ZAD1CS	ZRD	ADDRESS BUS A1=A0	ADRST VIA U51 (ALD)	FUNCTION
1)	$\overline{HOLD}$	$\overline{CS}$	$\overline{RD}$	A0	RST	
		X	X	*	0	Hold & Start Convert
2)	X	0	0	1	1	Read Output Data
	1	0	0	0	0	Rd Status Reg.
	X	1	X	*	X	HI Data Bus
	X	X	1	*	X	HI Data Bus
	X	X	X	X	1	Reset
	0	0	X	0	X	Reset

ADC Control Signals
Figure 34

AC/DC input mux switch AC, DC, and validity signals to DC gain select and then send the signal to the ADC. 2WM1EN from U51, additional logic decode (ALD), enables 2A0 - 2A2, from the microprocessor through the output latches, to address proper inputs to select the DC gain for RADAL and RAVAL signals.

The DC gain select is used to expand low level inputs. The input signals are buffered and sent through U14A and U15A. U14A and U15A normally have a gain of 1. Control signals IZ5PG1 and IZ5PG2 from the microprocessor select how much the gain of operational amplifiers AR12 and AR13 are by changing the feedback loop impedance. If more gain is required for RADALT signal, U14A is deenergized and R157 is included in the feedback loop for AR12 making the gain 3.9. The same type of circuit is used for DC selection of RAVAL. The output of DC gain select is sent to the submux circuits.

Submux circuits switch inputs from AC/DC or synchros to the ADC. Switches U14B and U15B are controlled by signal 3Z2SEL from the microprocessor. With a 0 on 3Z2SEL, AC/DC input muxes are selected. The input limiter circuit clamps any input to the ADC to ±5.25Vdc to prevent any damage to the ADC, U21.

ADCs U21 and U22 are 14-bit 'self-calibrating' converters operating in bipolar mode. BP/UP is tied to VD +5V to ensure bipolar operation is selected. The signal input to AIN must not exceed ±5.25Vdc. The input limiter circuit ensures this requirement is met. Figure 34 shows the relationship of control signals and ADC operations.

NOTE: *The status of bit A0 is not critical to the operation specified. However, A0 should not be low when CS and HOLD are low, because a software reset is sent to the microprocessor if both signals are low.*

To coordinate the sequence of ADC control signals, the following paragraphs describe what state each signal is in to produce data conversion.

In Figure 34, the number 1 shows what the control lines are for the microprocessor conversion start. When the conversion is complete, signal end of conversion (EOC) (pin-

42) informs the microprocessor, through the program discrete input buffers, that conversion is complete. Signal end of track (EOT) (pin-41) informs the microprocessor when enough time has elapsed since the last conversion for ADC to acquire a new analog signal.

Number 2 shows what the control lines are as the microprocessor reads the digitized data. Data is in twos complement with the most significant bit (MSB) inverted. The MSB is data bit 15 (A4). Software corrects this discrepancy. The output is +5.25Vdc and is sent to the ADC data bus buffers.

ADC data bus buffers U17 and U18 act as level shifters changing the 5.25Vdc output of the ADC converters to 5.00Vdc out to be compatible with the logic devices. ZADRD from the gate array controls the output.

The microprocessor transfers data to the ADDA RAM, U59 MSB and U60 LSB. ADDA RAM acts as a scratch pad and memory stack. Scaling of the data is done in the RAM, preparing the data to be transferred to the PVM through the dual port RAM (DPR).

(14) Dual Port Ram Interface

This interface consists of buffer line driver U50 and bidirectional transceivers U48 and U49. U50 is kept constantly enabled by having G1 and G2 control lines tied to ground. This buffer is always enabled to allow constant communication between the ADDA and PVM boards.

Signal Y8 (pin-11) goes to the PVM as ZDPRAM and is used to enable the ADDA portion of the DPR ($\overline{\text{MCS0}}$ from the microprocessor). Signal Y7 (pin-12) goes to the DPR as ZWR. ZRD is used to enable the output ($\overline{\text{OER}}$ on the DPR, pin-46) (RD from the microprocessor). Signal Y6 (pin-13) is ZWR. When ZWR is high, the DPR microprocessor reads data (ZRD must be low at this time). When ZWR is low, the microprocessor writes data to the DPR (WR from the microprocessor).

U48 and U49 are bidirectional transceiver ICs that interface with the DPR. The ICs are enabled with a combination of logic through the DPR buffer enable. This inverter/NAND combination provides faster switching, and ensures a valid read ($\overline{\text{RD}}$) or write (WR) from the microprocessor is present, when MCS0 from the microprocessor is also present.

The microprocessor data transmit/receive control also specifies if the transceivers receive (logic low) or transmit (logic high) data. These signals go to the ADDA from J17 to the PVM J7 connector.

Address line A0 through A11 are directly interfaced through ADDA J16/J15 to the PVM J8/J9. Signal ZDPRAMBSY from the PVM DPR (pin-49) to PVM J7 to ADDA J17 pin-4, goes to U51 ALD, pin-28, to inform the PVM microprocessor of a DPR busy condition, inserting a wait state into the microprocessor through the ARDY line.

(15) AC Signal Inputs

The AC Barorate #1 signal (ARINC 545A, 565) inputs to the ADDA come into the unit at the MKVII Backplane and then to the operational amplifier circuits on the ADDA. Following is a list of the signals:

INPUT SIGNAL	MKVII	INTERNAL	ADDA	AR9C(S5)
H	J1B - 37 - - ->	J5 - 7 - - ->	J12 - 7	Pin 9
L	J1B - 38 - - ->	J5 - 8 - - ->	J12 - 8	Pin 10
				AR9D(S5)
REFERENCE				
H	J1B - 39 - - ->	J5 - 5 - - ->	J12 - 5	Pin 13
L	J1B - 40 - - ->	J5 - 6 - - ->	J12 - 6	Pin 12

AR9C operational amplifier gain is 0.75. DG2 provides low impedance for the current when the MKVII power is off and also provides high voltage spike protection during operation. The output of AR9C is inverted and sent to AC/DC input mux.

The AC baro rate input comes into AR9D operational amplifier and it has a gain of 0.26. The reference inputs are used for scaling. If the reference voltage goes down, software scaling in the ADDA is adjusted to keep the scaling and the operation accurate. The output is 180° phase shifted and sent to the AC/DC input mux.

(16) AC Baro Reference

AC baro reference is also sent to the AC reference attenuators (S5). The signal is attenuated and sent to AC reference mux (U7 and U16). Signals RA0 through RA2 from the microprocessor through the output latches select which reference signal is sent to the zero cross detector.

(17) Zero Cross Detector

The zero cross detector informs the gate array of zero cross for AC synchro signals. It starts a timer to provide for sampling input signals at peak polarity. The signal is also sent to ground discrete input port (U33 and U38) to be used by the microprocessor to see phase relationship of the reference to AC/synchro signal.

NOTE: *No phase inversion of reference occurs, but the input AC signal is inverted. If REFINT is low and AC signal is measured, a positive polarity signal is considered 'in phase'.*

```
Reference + Signal = Same polarity = Out of Phase
Reference + Signal = Different polarity = In Phase
```

The input references to AR11C pins-11 and 12 are inverted and sent to the gate of MOSFET Q5 (n-channel enhancement). Q5 turns off and on depending on input polarity. Q5 output (ground or +5Vdc) goes to the gate array. The gate array looks for a voltage change for signal REFINT to tell the microprocessor when to sample the information on the data bus.

(18) Barorate Validity

The input from aircraft sensors goes to J1B pin-27 to J2 pin-9, the ADDA J9 pin-9 and finally to U39 pin-7. This +28Vdc discrete input (S8) signal is read by the microprocessor on the data bus, bit 5, looking for barorate validity status.

(19) Barorate Processing

Barorate processing follows the same electronic routine as the Radio Altitude DC signal input. The signal BRISAC comes in the U4 pin-4 (S6) and goes to the DC gain #1 circuit. The reference signal BRIRAC goes to U4 pin-13 (S6) and then to the DC gain #2 circuit.

(20) The Synchro Inputs

The AOA synchro signal from the sensor input to the MKVII rear panel connector uses the following inputs:

Input	BACKPLANE	ADDA
X axis	J2 H1 - - ->	J3 pin-2
Y axis	J2 H2 - - ->	J3 pin-3
Z axis	J2 H3 - - ->	J3 pin-4

NOTE: This synchro input does not use a validity or reference control.

The connectors on the ADDA (J1 - J8) are offset on the Backplane by +1 (e.g. ADDA J3 pin-2 goes to the Backplane J2 H1). This offset of the flex cables to the Backplane helps prevent ground loops.

(21) Input Mux

Switching the various synchro signals to the conversion buffers, signal Z3A3, enables mux #1. 3A0 through 3A2 specify which input is to be used. The outputs are sent to the conversion buffers through input buffers AR11A, AR11D, and AR11B. Initial synchro conversion uses internal MKVII analog ground.

(22) Conversion Buffers

AOA #1 XYZ inputs are sent to input mux #1, then multiplexed to buffer AR10C, which uses the formula 2-3, and to buffer AR10A, using the formula 1-3. AR10B output is cosine of summing the two equations.

AOA #2 uses the same scheme of input mux to the conversion buffers, but the formula is developed to cross compare between AOA #1 and AOA #2. The formula is (1 - 3) X (2 - 3) = Cosine reference. This cross compare ability of the MKVII allows for two channel synchros and guarantees that if one synchro input develops a problem, the unaffected AOA synchro can provide a correct output preventing an erroneous signal from being processed.

(23) Cosine Reference Summer

AR10B provides a cosine reference signal (cosine of input angle) to be used as a reference to the zero cross detector. This circuit is for synchros that do not have their own reference and is limited to synchros with inputs of 0 to $\pm 90^{o}$. The output is sent to AC reference attenuators and the zero cross detector (S5).

(24) AOA AC/DC Input Select

To select proper biasing for synchro or DC AOA, signal AOASEL from the microprocessor controls the n-channel enhancement MOSFETs Q1 through Q4. A high on AOASEL turns on Q1 through Q4 which then applies ground to X and Y input. Low on AOASEL turns off Q1 through Q4 providing high impedance to the DC inputs which go to operational amplifiers AR5, AR6 (S4) for DC AOA processing. Resistors attenuate the 11.8Vac input from the rear panel connector to a level that is usable to the muxes.

(25) Program Pin Input

Program pins are ground seeking discretes (S7). Signals ZPP1 and ZPP2 from the gate array control input of discretes to the data bus. 16-bit data used by the microprocessor

and ADDA RAM, PVM DPR to check the configuration information.

(26) Discrete Inputs

Discrete inputs are divided into ground, +28Vdc, and programmable. The ground inputs are pull up. The signal ZDISCI from the microprocessor controls inputs to the data bus. REFINT is used by the microprocessor to determine polarity and phase relationship between reference and AC/synchro input and is also input as a ground discrete. The inputs are processed by the microprocessor at a 150 millisecond interval.

+28Vdc inputs are voltage divided to provide a +5.95Vdc input to buffers U39 and U40. Buffers further shift the level output to +5.00Vdc (these are clamped through internal diodes of high speed CMOS (HC) devices). The signal ZDISC2 from the microprocessor controls the inputs to the data bus. DOGSTS from the gate array is sent to the microprocessor status line of the ADDA 131 millisecond watchdog timer to indicate what kind of reset is asserted. Inputs are processed by the microprocessor at a 150 millisecond interval.

The programmable inputs are discrete inputs that can be either +28Vdc or ground. Signals PP1-Z+ and PPG-Z+ from the microprocessor control the inputs. If the signal is high, +28Vdc discretes are programmed using the voltage divider network as the +28Vdc discretes previously described. If the signal is low, ground discretes are programmed. The inputs are sent to buffers U45 and U46 to be put on the data bus. Signal ZDISC3 from the microprocessor controls these buffers. The inputs are processed at a 150 millisecond interval.

(27) ARINC 429/575 Digital Air Data System (DADS)

ARINC 429/575 inputs come into the unit on the following rear panel connectors:

```
INPUT #1

A = J1A - 17 - - ->    J4 - 13 - - ->   ADDA J11 - 11
B = J1A - 18 - - ->    J4 - 14 - - ->        J11 - 14
```

The inputs go through resistor attenuators to input switches U23 and U24 and to the 429 transceiver U36 (S9).

ARINC 429 Transceiver, U36, is a very large scale integrated (VLSI) 429 IC consisting of four independent ARINC receivers and one ARINC 429 transmitter. The transceiver interfaces to a micro controller through an 8-bit bi-directional data bus, 4 address lines, and 4 control lines. The device is programmable to accept either analog or digital input signals. The receivers are programmable for speed selection and automatic label recognition. The transmitter is programmable for speed selection.

All four receivers as well as the transmitter can be accessed and controlled independently by means of status and control registers. Additionally, a global main status register allows quick access to any information stored.

The receiver selection features programmable speed selection, error detection, and double frame input buffer. It is programmed to automatically toggle an output pin (interrupt line) upon recognition in the receive buffer of labels previously programmed in the receiver memory. Four valid label recognition flags, LHIT0-3, go to the gate array to inform the microprocessor of valid label. Up to 256 labels can be programmed into the very large scale integrated memory (VLSI).

(28) ARINC 429 Operation

A valid 429/575 word is input to VLSI on channel 1. $\overline{\text{RHIT0}}$ (pin-64) goes low to the gate array. The gate array informs the microprocessor through GINT to the microprocessor into pin-45. The microprocessor responds by setting INT2/$\overline{\text{TA0}}$ low, acknowledging the interrupt. Upon receipt, the gate array places a vector on the data bus. The microprocessor addresses ROM and executes the instructions. Z429CS and ZRD are set low by the microprocessor and the address lines A1 through A4 to read the correct channel. Data is output to U44, the transceiver. U44 is enabled by Z429EN signal through the 429 buffer enable logic. Also, U44 provides faster switching and isolation, and it ensures valid read or write and PCS3 signals before accessing the 429 VLSI.

The direction of the data is controlled by DTZR from the microprocessor. A high on TX input tells the transceiver to review its contents. A low TX input allows the 429 VLSI to output data.

GAP output ($\overline{\text{GAP0}}$ - $\overline{\text{GAP3}}$) goes low indicating ARINC bus activity. As lines go low, JK flip/flop U27 and U28 toggle. Data can be read by the microprocessor (U45) to verify lines are active. The signal ZACRST from the gate array resets the flip/flops in the ARINC 429 activity monitors.

The 429 test signal 429TST, a logic high from the microprocessor through the output latch U57, sets the 429 receiver into self test mode. First the switches U23 and U24 open to isolate the 429 VLSI integrated circuit (IC) from the inputs. U37 inverts 429TST high level to a low which turns off switches U25 and U26 (closed). This allows an ARINC 429 wrap around test pattern, set up by the microprocessor, which goes to VLSI TX high and TX low, to send them to the receiver inputs. Data is 'wrapped' to the receiver inputs by way of U36 ADINOH - ADIN3L. The data inputs and outputs are then checked by the microprocessor for validity and parity. ARINC 429 transmits data through the 429 VLSI single transmit channel. High and low data is sent to AR18B and AR18C where it is then transmitted out on rear panel connectors J2 - C10 (high) and J2 - C11 (low) to the DPR on the PVM.

(29) Miscellaneous Circuits

±5.25Vdc regulators (S2) provide voltage to the ADC circuits.

Biaxial test circuit (AR18A, S7) uses signals ACSTLO and ACSTLI from the microprocessor to program AR18A to output a ±6Vdc signal (minimum) to drive the biaxial accelerometer to the maximum deviation in each axis. The inputs to the MKVII are read and checked for accuracy by the microprocessor.

The internal reference buffer, AR20 (S7), provides isolation for VRef + 5Vdc to the operational amplifiers. The hold-up circuit provides two seconds of power to the RAM ICs in the event power is lost. The signal XZRST from the Power Supply is high during normal operation. XZRST turns on Q10 which applies ground to the base of Q13 which turns on and applies + 5Vdc to the RAM ICs. XZRST also turns on Q11 and Q12 to pass chip select signals (low) to the RAM to allow memory access. If power is lost, XZRST goes low. Q11 and Q12 turn off deselecting RAM. Q10 is off and turns Q13 off. C111 and C112 discharge, providing the voltage to the RAM to complete tasks in progress. CS lines go high to prevent any data from being partially written.

(30) Auxiliary Reference

VR1 provides a precision +2.5Vdc IC reference signal that is applied to AC/DC input mux U3 pin-10 and U5 pin-10. Address 2A2 = 1, 2A1 = 1, and 2A0 = 0 from the microprocessor

output latches switch signals through the mux. The 2.5Vdc reference is input and digitized and compared in U21 with values stored in ROM, U52. The microprocessor, U35, checks the ADC scale factor and voltage offset errors of both the ADC, U21 and U22.

(31) PVM Reference

The PVM U7 pin-6 produces a +5Vdc reference that is sent to the ADDA board. R137 and R138 act as a voltage divider network to reduce the +5Vdc to precisely +2.5Vdc reference for U6, mux 1B. Addresses 2A2 = 0, 2A1 = 1, and 2A0 = 1, from the microprocessor set the output latches to switch the input signals through U7 mux. This circuit also acts as check on the PVM reference voltage through ADDA U22 ADC.

(32) Isolation Diodes

Diodes (D6 through D9) provide isolation on four of the discrete inputs (flap, gear, glideslope, and audio suppress) to guard against sneak circuits on the aircraft.

D. PVM Board

Figure 35 shows a block diagram of the PVM board.

(1) Hardware/Software Interface

The PVM microprocessor is a 16-bit Zilog Z8002A, with a clock speed of 6mHz. For detailed information about the microprocessor, see the Zilog 'Z8000 Technical Manual' and/or the AMD 'MOS Microprocessors and Peripherals' Databook. A number of memory and input/output (I/O) devices are available to the microprocessor.

(a) Memory devices are:

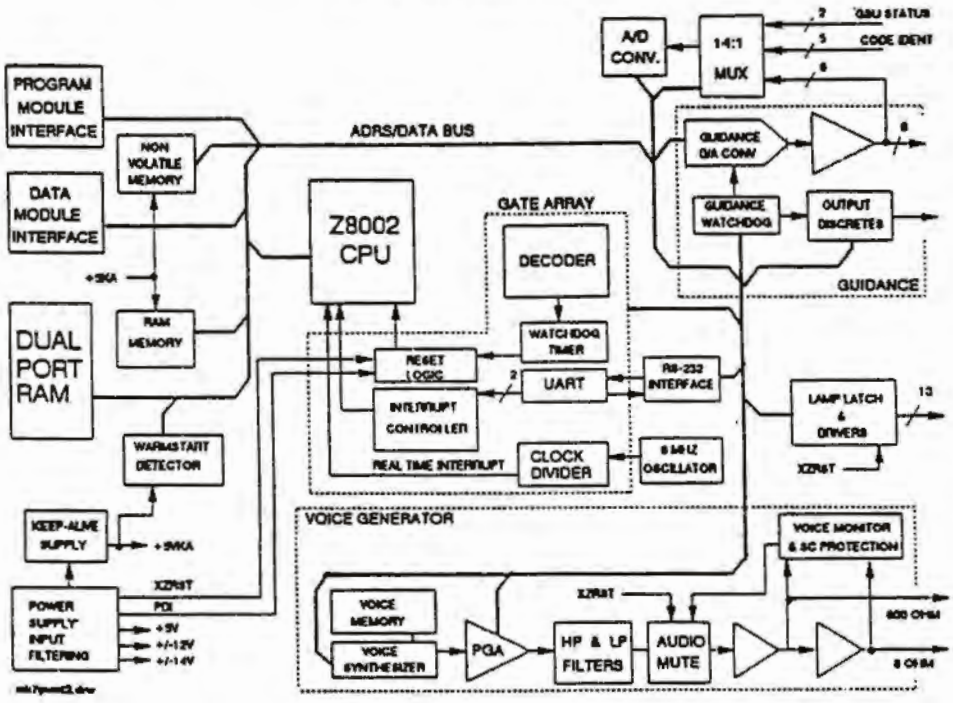
```
Random access memory (RAM)
Data Module memory
Program Module memory
Dual port RAM memory
```

(b) I/O devices include:

```
Nonvolatile memory (NVM)
Lamp drivers
Voice synthesizer
ADC converter
UART interface
Miscellaneous inputs port
Analog input multiplexers for the ADC
Voice volume control port
Interrupt controller interface
Guidance command digital-to-analog converter (DAC)
Various monitor and test circuits
```

(2) Microprocessor Operation

From pin-8 of U28D, a low signal goes to the microprocessor pin-11 as VI. This 82 microsecond delay is to assure the microprocessor has proper vector interrupt timing. The microprocessor responds by setting the status lines, ST0 - ST3, to send the gate array the signal INT.ACK. Between the microprocessor and the gate array, the gate array sends interrupt vector signals, and the microprocessor processes these interrupts ac-



PVM Block Diagram
Figure 35

cording to their priority rating. RESET is ZRESET signal from the gate array and is the result of XZRST from the power supply, or watchdog timeout, or the removal of a program or data module.

ZWAIT signal is sent from the gate array to the microprocessor telling the microprocessor that the gate array, or any device interfaced with the gate array, is not ready for the microprocessor input. The gate array interfaces devices such as the voice chip U30, 8 bit ADC U2, or DPR U37. ZWAIT puts the microprocessor in a wait state.

(a) Microprocessor Wait States

The microprocessor can insert wait states when reading and writing to various memory and I/O devices. All memory devices listed previously operate with no wait states. The Z8002 microprocessor automatically inserts one wait state for all I/O devices. Wait states are added by the microprocessor when required; this is controlled by the ZWAIT signal, which is generated by the gate array. The number of wait states denoted in the memory map refers to extra (1, 2, or 3) wait states added to the normal I/O cycle time. The memory map is shown in TESTING AND TROUBLESHOOTING.

(b) Microprocessor Clock Frequency

Y1 provides 6mHz clock for the microprocessor. Output of inverter U28C gives the Gate Array ZCLK signal.

(c) Microprocessor Signals

Data strobe ($\overline{DS}$) is a 'times in/out' of data to the gate array from the EMD. Byte/$\overline{Word}$ (B/$\overline{W}$, BZW) defines memory references on the address/data bus. This signal goes

to the EMD, U38, and the gate array. Status lines, ST0 through ST3, specify what the microprocessor status is, such as interrupt, transferring data, etc.

Non-maskable interrupt ($\overline{NMI}$). The signal input XPINT is from the power supply. XPINT is then inverted by open collector NAND gate, U10D.

Non-vectored interrupt ($\overline{NVI}$). The signal is ZNVI from the PVM gate array. This is a 4.096-millisecond interrupt that establishes the PVM software/timing cycles.

Vectored interrupt (VI) is a signal from the gate array. A group interrupt signal ZGINT from the gate array, delayed 82 microseconds by U44, is used to divide the 6mHz ZCLK signal. When ZGINT transitions to a low, after a delay of 82 microseconds, the output pin-14 of U44 goes high and is inverted by U28D.

(3) Address Latches

U41 and U43 are controlled by the microprocessor. Signal $\overline{AS}$ is inverted by U28A to produce control line ALE. Data latches U40 an U42 are enabled by ZDBUSEN, developed by U38, direction controlled by microprocessor R/$\overline{W}$ select.

(4) Extended Memory Decode

U38 is an EP900 electronically programmable logic device (EPLD) used as a memory and chip decoder. It uses control and status lines from the microprocessor, various address lines, and Z138A signal from the gate array to provide chip select and enable logic to various PVM circuits.

(5) Watchdog Timer

The watchdog timer is driven from the system clock, and it times out if not reset every 131.072 milliseconds. The effect of a timeout is that the PVM hardware and software are reset and re-started.

(6) Program Module

The program module can be inserted and removed from the unit while power is applied. Removal is sensed by the PVM, and +5V is switched off from the module, before the module becomes disengaged from the connector.

```
SIZE:  32K X 8 EACH
ADDRESS:  0000 - FFFFH, CODE SPACE
0000 - 7FFFH, DATA SPACE
0000 - FFFFH, SPECIAL I/O SPACE

DATA WIDTH:  16 BITS
WAIT STATES:  ZERO IF EXECUTING CODE
ONE AUTOMATICALLY IF SPECIAL I/O OPERATION (CHECKSUM)
```

(7) Data Module

The data module can be inserted and removed from the unit while power is applied. Removal is sensed by the PVM, and +5V is switched off from the module, before the module becomes disengaged from the connector.

```
SIZE:  32K X 8 EACH
```

ADDRESS: 8000 - FFFFH, I/O SPACE
DATA WIDTH: 16 BITS
WAIT STATES: ONE (AUTOMATICALLY INSERTED FOR I/O TRANSACTIONS)

(8) RAM Memory

SIZE: 8K BYTE EACH (8K WORDS TOTAL, EXPANDABLE TO 16K WORDS)
ADDRESS: 9000 - FFFFH, DATA SPACE
DATA WIDTH: 16 BITS
WAIT STATES: ZERO

(9) Nonvolatile Memory

SIZE: 8K BYTES
ADDRESS: 1001 - 4FFFH, ODD ONLY, NORMAL I/O SPACE
ENDURANCE: 100,000 CYCLES / BYTE

DATA RETENTION: 10 YEARS
WAIT STATES: ONE ADDED AUTOMATICALLY FOR I/O TRANSACTIONS
WRITE CYCLE TIME: 1 millisecond

(10) Dual Port RAM

IDT 7142 SLAVE DPRAM CHIP
SIZE: 2K X 8 EACH
ADDRESS: 8000 - 8FFFH, DATA SPACE
0000 - 0FFFH , I/O SPACE (UNUSED)

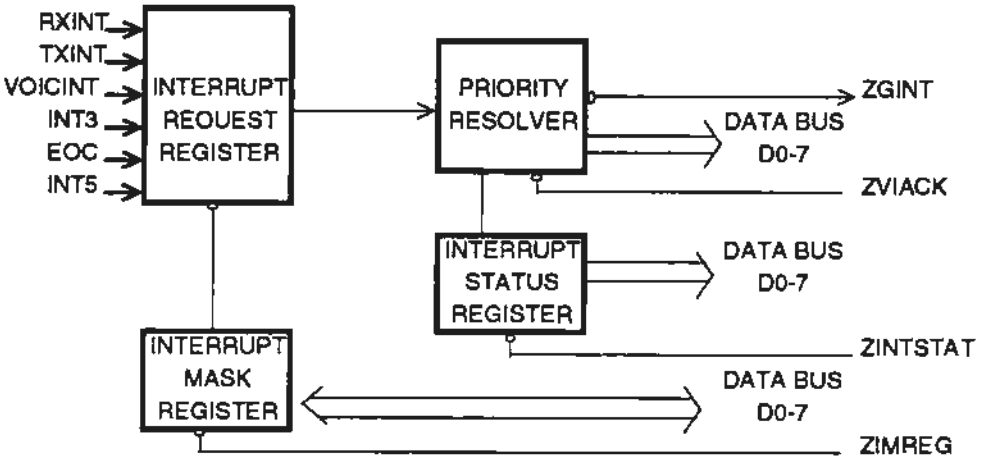
DATA WIDTH: 16 BITS
WAIT STATES: ZERO IN DATA SPACE
ONE IN I/O SPACE

The master and slave RAM devices are identical, except that the bus arbitration scheme is controlled by the master device.

(11) Interrupt Controller

A block diagram of the interrupt controller architecture (implemented in the gate array) is shown in Figure 36.

The interrupt controller has 6 active high inputs latched by the interrupt request register. All are maskable through the interrupt mask register, which employs a fixed priority scheme, in which the RS232 interrupt is the highest priority and INT5 is the lowest. The signal ZGINT is an active low output asserted whenever one or more pending interrupts are asserted. The interrupts are serviced when the Z8002 microprocessor executes a vectored interrupt acknowledge cycle in response to the low level on its ZVI pin. The gate array decodes the microprocessor status lines to detect a VIACK cycle in progress. When a VIACK cycle is detected, the interrupt controller drives the data bus with a vector value, which computes the address of the service routine for an interrupt input.



Interrupt Control Scheme
Figure 36

The interrupt channels are assigned as follows:

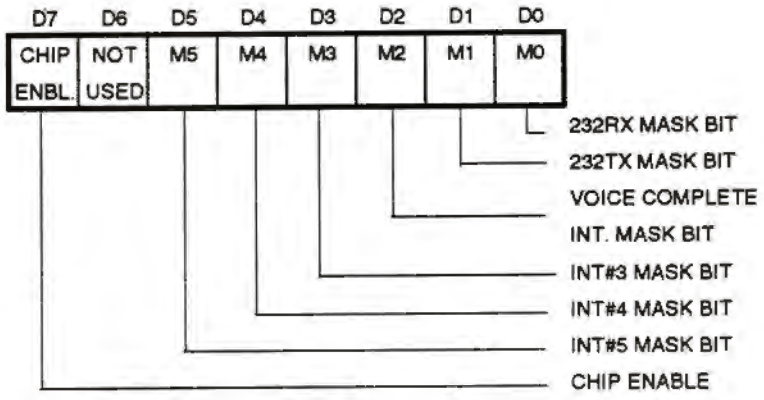
INT#	FUNCTION	SPECIAL INSTRUCTIONS
(0)	RS232 RCVR:	If INT is latched while mask BIT is disabled, an INT is asserted immediately after mask is enabled.
(1)	RS232 XMTR:	BIT in INT status register is set 53 microseconds early. ZGINT signal is delayed by 53 microseconds in hardware. Requires SW FIX.
(2)	MSG COMPLETE:	Don't enable INT mask until 10 microseconds after output voice.
(3)	SPARE	
(4)	ADC CONV EOC:	Indicates ADC conversion is completed.
(5)	SPARE	

(12) Interrupt Request Register

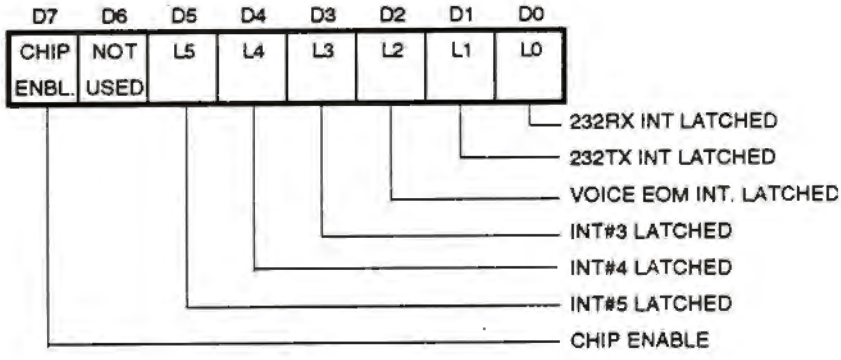
The interrupts at the INT# input pins are logically ANDed with the corresponding bits in the interrupt mask register, then latched as pending interrupts. This register is cleared by an active-low ZRESET input.

(13) Interrupt Mask Register (Adrs = 5141H, NIO Space, Read/Write)

An 8-bit mask value is written to this register to enable the device and allow interrupt inputs to be latched. The register can be read for test purposes. This register is cleared to 00H by an active-low ZRESET input. A '0' masks the interrupt, and a '1' enables the interrupt input. Refer to Figure 37.



Interrupt Mask Register Bit Format
Figure 37



Interrupt Status Register Bit Format
Figure 38

(14) Interrupt Status Register (Adrs = 5161H, NIO Space, Read only)

This register allows reading the state of all of the interrupt input latches. A '1' indicates that the interrupt is pending and needs to be serviced. This register reads 00H after an active low ZRESET input. Refer to Figure 38.

(15) Vector Data During Acknowledge Cycle

This signal is on the data bus during VIACK cycle.

The 3 least significant bits of the vector value are decoded to determine the highest priority pending interrupt. If more than one interrupt is pending, the highest priority input is serviced first. Refer to Figure 39.

(16) Miscellaneous Input Buffer (Adrs = 5081H, NIO space, Read only)

Vector Interrupt Data Bits

HIGHEST-PRIORITY PENDING INTERRUPT	D2	D1	D0
232RX INT.	0	0	0
232TX INT.	0	0	1
VOICE INT.	0	1	0
INT#3	0	1	1
INT#4	1	0	0
INT#5	1	0	1

Vector Interrupt Data
Figure 39

Miscellaneous Input Buffer

D0 = RSTSTS	(0 = PWR SUPPLY	1 = WDOG TIMEOUT)
D1 = ADIFLAG1	(0 = IN VIEW	1 = OUT OF VIEW)
D2 = ADIFLAG2	(0 = IN VIEW	1 = OUT OF VIEW)
D3 = GUIVAL	(0 = GUIDANCE FAULT	1 = VALID)
D4 = SWUMDN	(0 = 28V BUS FAULT	1 = OK)
D5 = WARMSTART	(0 = COLDSTART	1 = WARMSTART)
D6 = Z600VAL	(0 = OK	1 = 600 OHM AUDIO FAIL)
D7 = Z8VAL	(0 = OK	1 = 8 OHM AUDIO FAILURE)

Miscellaneous Input Buffer
Figure 40

Refer to Figure 40.

(17) Discrete Outputs (Adrs = 5001H, NIO space, Write only)

Refer to Figure 41.

NOTE: *The state of the lamps are latched. The latches are reset to 0 under any of the following conditions:*

Power Supply fault
Watchdog timeout
Data Module not installed
Program Module not installed
Guidance Watchdog timeout
GSU #1 = faulty
GSU #2 = faulty

The ADI flags are driven out of view if none of the previously listed conditions exist. Also, the guidance 'select' and 'deselect' signals can only be asserted if none of the previously listed conditions exist. In this way, the guidance outputs are 'interlocked' by the validity circuits, and inhibited if the MKVII or the GSU is inoperative.

Discrete Outputs Data Bits

BIT NOMENCLATURE	REAR CONN #	STATE
D0 = GLIDESLOPE ALERT LAMP	(J1A-21) 0 = OFF	1 = ON
D1 = GLIDESLOPE CANCEL LAMP	(J1B-33) 0 = OFF	1 = ON
D2 = GPWC LAMP	(J1B-11) 0 = OFF	1 = ON
D2 = SPARE	(J1B-9)	
D2 = SPARE	(J1A-13)	
D3 = GPWC INOP. LAMP	(J1B-12) 0 = ON	* 1 = OFF
D4 = AUTO. BACKCOURSE ANNUNC.	(J1B-10) 0 = OFF	1 = ON
D5 = WS PRE-ALERT LAMP	(J2-1A) 0 = OFF	1 = ON
D6 = WINDSHEAR WARNING LAMP	(J2-2A) 0 = OFF	1 = ON
D7 = WS SYS. FAILURE LAMP	(J2-3A) 0 = ON	* 1 = OFF
D8 = SPD. CMD. TAKEOFF MODE	(J2-15B) 0 = OFF	1 = ON
D9 = GUID GSU DE-SELECT #2	(J2-14B) 0 = OFF	1 = DESEL.
D10 = SPD. CMD. GO-AROUND	(J2-13B) 0 = OFF	1 = ON
D11 = GUID GSU SELECT #2	(J2-12B) 0 = OFF	1 = SELECT
D12 = FLT. DIRT OFF SELECT	(J2-11B) 0 = OFF	1 = SELECT
D13 = GUID GSU DE-SELECT #1	(J2-7B) 0 = DFF	1 = DESEL.
D14 = CAPT ADI FLAG	(J2-11A) 0 = VIEW	1 = UNSEEN
D15 = 1st OFFICER'S ADI FLAG	(J2-5B) 0 = VIEW	1 = UNSEEN

Discrete Outputs Data Bits
Figure 41

(18) Voice Interface (Adrs = 5181H, 5701H, 50E1H, 5021H, NIO Space)

The MKVII Warning Computer voice circuit uses an NEC PD7759 LSI chip and two 1 MBIT EPROM devices. The NEC chip contains all of the logic necessary to decode and extract data from the voice EPROMs, as well as a 9-bit DAC and delta modulation hardware to produce an analog audio signal. The NEC chip provides 3 sample rate options. Some words can be encoded at a high sample rate, others medium or low sample rate in the same EPROM. The physical location of each word in EPROM is determined automatically at encoding time and is transparent to the host system. The communication between the PVM system software and the NEC chip is very simple. The NEC chip asserts a /BUSY signal (low) within 10 microseconds after the write cycle. This /BUSY signal is connected to interrupt #2. When the voice output is complete, a low to high transition occurs on the /BUSY line. Since the interrupt controller has active-high inputs, the interrupt input is disabled when the voice circuit is not being used.

(19) Voice Annunciation

The following sequence is used by the voice circuit to produce an annunciation.

1. Write to Adrs. = 5181H to reset the voice chip
2. Wait at least 20 microseconds
3. Write to Adrs. = 5701H to enable to voice chip
4. Write loudness value to the programmable gain amplifier Adrs = 50E1H (00H = Mute, FFH = Max.)
5. Wait at least 8 msec.
6. Write Message # (0 - 511) to the NEC chip Adrs = 5021H, Word Mode.

7. Wait at least 10 microseconds.
8. Enable Interrupt #2
9. When Interrupt #2 is serviced, be sure and disable it.

NOTE: All address values given are in normal I/O space. Message number values must be written in 'word mode'.

(20) Voice Menu

The voice circuitry produces the following words as shown in Figure 42.

(21) Mux Channels (Adrs = 50C1H, NIO space, Write only)

The selection of the mux channel is the result of the MKVII writing data to Adrs = 50C1H. Refer to Figure 43.

(22) Reading Hardware Version Resistors

When the MKVII reads the hardware version resistor values, the following formula computes the resistance value:

$$R = \frac{256 * 104 * (D - D')}{(256 - D) * (256 - D')}$$

where: R is in ohms
D' = Data read from Chan #0
D = Data read from Chan #n
n = (1,2,3,4,5)

(23) Reading Guidance Wraparound Voltages

When the MKVII reads the guidance command voltages, the following equations are used:

The basic transfer function for no-load conditions is:

DAD = (DDAC/16.7) + 7.2

The transfer function with an ADI load connected is:

DAD = (DDAC/16.7)(1 + 1K/RL) + 7.2 - 122K/RL

The value of the ADI load is a function of the data written to the DAC and the data read from the ADC, the following equation:

$$R_{load} = \frac{(512 - DDAC) * Rs}{DAC - (4 * DAD)} \quad Ohms$$

where: Rs = 1000 ohms
DDAC = Data output to DAC
DAD = Data read from ADC

This equation is invalid for: (DDAC - 4*DAD) <10. The guidance output voltage is a function of ADC data read, and the following equation is used:

VO = ([(127 - DAD) / 12.5] * [RL / (1K + RL)])

(24) Reading GSU Validities

The ADC converter and muxes are in an indeterminate state at power-up. The muxes require 2 microseconds (worst-case) settling time, and the ADC can complete a conversion within 100 microseconds. An 'end-of-conversion' interrupt (EOC) is provided to facilitate

MSG	MESSAGE	MSG	MESSAGE	MSG	MESSAGE	MSG	MESSAGE
00	NULL	2B	FIFTY	111	RADIO	13C	THRUST
01	A	2C	FIVE	112	RATE	13D	TEST PULSE
02	ALPHA	2D	FLAP	113	RIGHT		
03	ACCELEROMETER	2E	FLAPS	114	ROLL		
04	AHEAD	2F	FLIGHT	115	RUNWAY		
05	AIR	30	FORTY	116	SEVEN		
06	AIRSPEED	31	FOUR	117	SEVENTY		
07	ALTITUDE	32	GEAR	118	SHEAR		
08	ANGLE	33	GLIDESLOPE	119	SIX		
09	APPROACH	34	GROUND	11A	SIXTY		
0A	ATTACK	35	GUIDANCE	11B	SINKRATE		
0B	ATTITUDE	36	HEIGHT	11C	STALL		
0C	AUTOPILOT	37	HISTORY	11D	SWITCH		
0D	B	38	HUNDRED	11E	SYSTEM		
0E	BAKER	39	INACTIVE	11F	TEEN		
0F	BANK	3A	INOP	120	TEMP		
10	BARO	3B	INVALID	121	TEN		
11	BUSS	3C	LATITUDE	122	TERRAIN		
12	C	3D	LEFT	123	THIRTEEN		
13	CHARLIE	3E	LOCALIZER	124	THIRTY		
14	CANCEL	3F	LONGITUDE	125	THOUSAND		
15	CAUTION	40	MACH	126	THREE		
16	CHANGE	41	MAG TRACK	127	TOO LOW		
17	CHANGED	42	CALM WINDSHEAR	128	TURBULENCE		
18	CLIMB	43	HOOK	129	TWELVE		
19	COMPUTER	44	OUT	12A	TWENTY		
1A	COURSE	100	MARGIN	12B	TWO		
1B	D	101	MINIMUMS	12C	VERSION		
1C	DOG	102	MODULE	12D	WARNING		
1D	DATA	103	NINE	12E	WARNINGS		
1E	DECISION	104	NINETY	12F	WIRING		
1F	DON'T SINK	105	NO	130	WINDSHEAR		
20	E	106	NUMBER	131	ZERO		
21	ECHO	107	OF	132	0.75S QUIET		
22	EIGHT	108	OKAY	133	SIREN		
23	EIGHTY	109	ONE	134	700 HZ		
24	ELEVEN	10A	PINS	135	960 HZ		
25	F	10B	PITCH	136	1400 HZ		
26	FEET	10C	POINT	137	2800 HZ		
27	FOX	10D	POSITIVE	138	WHOOP		
28	FAULT	10E	PROGRAM	139	PLATFORM		
29	FAULTS	10F	PROX	13A	RECOVER		
2A	FIFTEEN	110	PULLUP	13B	REDUCE		

Voice Menu Words
Figure 42

faster throughput. An active high interrupt (INT #4) is available to indicate that the ADC converter has finished the current conversion, and data is available to be read.

DATA	INPUT CHANNEL
00	10.0K CALIBRATION RESISTOR
01	P/S MOD. RESISTOR (RPOWER)
02	ADDA MOD RES. #1 (RADDA1)
03	ADDA MOD RES. #2 (RADOA2)
04	PVM MOD RES. #2 (RPV2)
05	PVM MOD RES. #1 (RPVM1)
06	F/O ROLL CMD. READBACK
07	WARMSTARTB SELF-TEST STATUS
0E	F/O PITCH CMD. READBACK
16	CAPT. ROLL CMD. READBACK
1E	CAPT. PITCH CMD. READBACK
26	FIRST OFFICERS GSU VALIDITY
2E	CAPTAINS GSU VALIDITY
36	F/O FAST/SLOW READBACK
3E	CAPT. FAST/SLOW READBACK

Mux Channels, Address 50C1H
Figure 43

(25) Guidance Interface

There are 3 types of commands issued from the MKVII to the Captain and First Officer ADIs through the GSU: analog command voltages, ADI flag outputs, and GSU select/deselect signals.

(26) Pitch, Roll, Fast/Slow Outputs (Adrs=5209H,520BH,520DH, 520FH, NIO space, Write only)

Pitch, Roll and Speed commands drive the Flight Director bars and speed bug of the ADIs. There are separate outputs for the Captain and First Officer display, and each output driver provides a ±5-Volt DC signal with RL >1000 Ohms.

NOTE: *Circuit is capable of ±10V DC with no load. These outputs are generated all the time, even when they are not connected to the ADIs.*

1. The MKVII pre-loads each of the DAC input buffers.

2. The MKVKII Writes DATA to Adrs = NNNN; writes command data to the input buffer of DAC channel using the following criteria:

Where: DATA = 204.8 * (10 - Vout) + 8 LSB; 4.883 mV / LSB
00H - BFFH range
Vout = Desired output voltage in Volts; (-5V to +5V)
NNNN = Adrs. of the Desired Channel as follows:

GUIDANCE OUTPUT	NNNN
PITCH COMMAND	= 5209 HEX
ROLL COMMAND	= 5208 HEX
FAST/SLOW CMD.	= 5200 HEX
Spare output	= 520F HEX

3. The data is strobed into the DAC output registers:

   Writes Data = FFH to: Adrs. = 7FFFH (NIO SPACE)

(27) ADI Flag Outputs (Adrs = 5001H, NIO Space)

The flag signal is independently generated on both PVM and ADDA boards, then wire ANDed together to drive logic-level signals for the flight director (FD) flags on the ADIs (Capt. and F/O) through the GSU. As a result, when the ADIs are connected to the MKVII, the flags can be driven out of view only if all of the following conditions are satisfied:

The GSU(s) are valid.
The PVM processor is failure-free.
The guidance watchdog timer has not timed out.
The ADDA board is also failure-free and commands flags out of view.

The data is written to the LAMPPORT: Adrs. = 5001H (NIO SPACE)

Where: DATA bit D14 = CAPTFLAG (1 = OUT OF VIEW, 0 = IN VIEW)
DATA bit D15 = FOFLAG (1 = OUT OF VIEW, 0 = IN VIEW)

(28) GSU Select/Deselect Outputs (Adrs = 5001H, 5301H, NIO Space)

The outputs command the GSU(s) to connect and disconnect the outputs from the MKVII to the Capt. and F/O ADI displays. A single wire, active high (+5V) signal (GUIDSTART) commands the GSU to select guidance for the ADI displays. A complementary active low deselect signal commands the GSU to restore the connection between the flight director system and the ADIs. Both signals are inhibited unless all the following conditions are satisfied:

The GSU(s) are valid.
The PVM processor is failure-free.
The guidance watchdog timer has not timed out.
The ADDA board is also failure-free and commands flags out of view.

NOTE: The deselect signal is wire-OR'd with the TOGA button in the cockpit, and an off-cycle detector in the GSU, so that the pilot can override the system and manually disconnect the MKVII from the ADIs.

This signal is monitored by the ADDA to ensure the following commands are carried out when the pilot selects to override the MKVII:

SELECT #1: 1. Writes DATA = FFH to: Adrs. = 5301H (NIO SPACE)
2. Waits 100 msec.
3. Writes DATA = 00H to: Adrs. = 5301H (NIO SPACE)

A 100 msec high select pulse is sent to the GSU #1 (J2-9A).

SELECT #2: 1. Writes to Adrs=5001H, and sets bit #11 = 1
2. Waits 100 msec.
3. Writes to Adrs=5001H, and clears bit #11 = 0

A 100 msec high select pulse is sent to GSU #2 (J2-12B).

DESELECT #1:
1. Writes to Adrs=5001H, and sets bit #13 = 1
2. Waits 100 msec.
3. Writes to Adrs=5001H, and clears bit #13 = 0

A 100 msec low deselect pulse is sent to GSU #1 (J2-7B).

DESELECT #2:
1. Writes to Adrs=5001H, and sets bit #9 = 1
2. Waits 100 msec.
3. Writes to Adrs=5001H, and clears bit #9 = 0

A 100 msec low to deselects pulse is sent to GSU #2 (J2-14B).

(29) Reset Behavior

The DAC outputs are reset to 0.00V by the microprocessor reset (ZRESET) signal. The rest of the guidance is reset either by the microprocessor reset condition or by the guidance watchdog timer timing out.

The guidance select signals are reset to the nonactive low state. The guidance deselect signals are reset to the nonactive high state. All flags are reset to the in-view low state. The flight director mode select discretes (FDGASEL, FDOFFSEL) are reset to the non-active low state.

(30) GSU Validity

Each GSU has a status output that is monitored by the PVM. For the MKVII to determine the status of GSU #1, it selects mux channel #2E and reads the ADC converter.

GSU STATUS	VOLTAGE AT REAR CONNECTOR	MIN DATA	MAX DATA
INVALID	0 <V <2.5	FF	6A
VALID AND DESELECTED	2.5 <V <7.5	6B	40
VALID AND SELECTED	7.5 <V <28	41	0

(31) Guidance Watchdog Timer (Adrs = 5409H, NIO Space, Write only)

The watchdog timer state is monitored at the miscellaneous input buffer (Adrs = 5081H), bit #D3. If the state of the bit is low, then the guidance hardware is inoperative. The guidance watchdog timer must be refreshed every 100 milliseconds or less. This is done by alternately having a 1 and a 0 written to data bit D3 on alternate writes to the guidance watchdog timer as shown in the following:

1. Writes Data = FFH to: Address = 5409H
2. Writes Data = F7H to: Address = 5409H
3. Go to step 1.

(32) Guidance Wraparound

Pitch and roll command outputs are read back through the ADC for MKVII test purposes.

Expected read back value is different (more) than the value commanded if a load is connected. The valid load range is 1000 ohms to 50,000 ohms. If the load impedance is less than 1K ohms, the amplifier output voltage range must be derated (from ±5V). If the load impedance is greater than 50K ohms, the read back circuit resolution is insufficient to reliably determine if the load is connected.

(33) Warmstart Detector and Power Down Interrupt

The warmstart detector is Address = 5501H, 5081H, NIO Space. The warm- start detector is built around an R/C discharge circuit, a comparator, a latch, and a transistor switch. When +5V power to the PVM board is lost, the R/C timing circuit begins discharging. If power is restored within 1 second, the output of the comparator remains a logic '1'. If the +5V power dropout exceeds 1 second, the comparator output goes low. In either case, when power is restored, the bit latched is read through the miscellaneous input port (address = 5081H, Bit #5, I/O Space). The detector is reset at power up and armed by writing 01H to address = 5501H, I/O Space. The warmstart detector is tested by writing 00H to address = 5501H, waiting for time T, then writing 01H to address = 5501H. The warmstart bit is read from address = 5081H.

```
If T <0.6 seconds, the value of the bit is '1'.
If T >1.6 seconds, the value of the bit is '0'.
If 0.6 <T <1.6 seconds, the value is indeterminate.
```

If a +5V dropout of duration T2 occurs, when power is restored, T1 initiates a warmstart detector test. The result of the warmstart detector test results in either a warmstart or a coldstart unit initialization and that choice equals the combination of T1 + T2 milliseconds. The error response is biased toward a coldstart. The value of T1 is saved in NVM at power down and the difference between 0.7 seconds and 1.6 seconds is corrected in the software.

(34) Power Down Interrupt

The power supply provides an early warning signal to alert the microprocessor that 115Vac power is going down. This signal is connected to the NMI pin of the microprocessor. Therefore, the NMI routine has provisions for saving critical restart data. On power down, the XPINT signal goes active high approximately 10 milliseconds before the XZRESET signal is asserted. Upon power up, the XPINT signal goes inactive slightly before the XZRESET signal goes inactive.

The MKVII procedure at power up is as follows:

The microprocessor reads address = 5081H (I/O), the miscellaneous input port.

If bit #0 = 1, the unit performs a coldstart (watchdog timeout).

If bit #5 = 1, the unit performs a coldstart test (T >1 second).

If the test fails, the unit performs a coldstart and then tests the warm-start detector. To perform a warmstart test, the microprocessor arms the warmstart detector by writing 01H to address 501H (I/O) and waits 4 milliseconds for C101 to charge up. The microprocessor then writes 00H to address = 5501H (I/O) and waits T <0.6 sec. The microprocessor rearms the detector by writing 01 to address = 5501H. The microprocessor then reads address = 5081H (I/O).

If bit #5 = 0, the PVM NVM indicates a coldstart has been initialized. After the coldstart is successful, a warmstart test is performed. The microprocessor writes 01H to address

= 5501H to arm the warmstart detector. It waits 4 milliseconds for C101 to charge up, then writes 00H to address = 5501H (I/O). Waits T >1.6 seconds. The microprocessor latches the value and rearms the detector by writing 01 to address = 5501H. It then reads Adrs=5081H (I/O).

If bit #5 = 1, that information is stored in NVM and coldstart power up is performed. Then the microprocessor writes 01H to address = 5501H to arm the warmstart detector.

(35) UART Interface (Address = 5061H, NIO Space, Read/Write)

```
Baud Rate = 19.2 ±0.5 Kbits/sec.
Starts bits = 1 (low level)
Stops bits = 1 (high level)
Data bits = 8
```

The UART is contained within the MKVII ASIC device, with the exception of the analog inputs and output driver. The UART is initialized at power up, and requires no programming. However, interrupts 0 and 1 of the interrupt controller must be enabled.

(36) Receiver

```
Valid '1' = Vin >2.0 Volts - Vih(min)
Valid '0' = Vin <0.8 volts - Vil(max)
```

Input Impedance is greater than or equal to 3.3K ohms.

Receiver port address: 5061H, Normal I/O Space (READ) Wait States: ZERO

Reception of a valid RS232 character causes an interrupt #0 to be generated by the UART. Since the receiver is double buffered, the data can be unloaded while the next character is being received (within 520 microseconds).

The receiver must be read within 520 microseconds after the interrupt is asserted; if it is not, the old data is overwritten by the new data. No overrun or framing error protection is provided, and no error annunciation is given. If a framing error occurs, the UART can become 'lost'. The UART must then be reset by asserting the ZRESET signal to the MKVII ASIC device, or applying a high input to the serial receiver of greater than 625 microseconds.

(37) Transmitter

```
V high (min) = 4.5 Volts
V low (max) = 0.2 Volts
```

Transmitter Port Address: 5061H, Normal I/O Space (WRITE) Wait States: ZERO

(38) Transmitting A Character

To transmit a character on the RS232 bus, U19 (the gate array) performs the following steps:

1. It enables interrupt #1.
2. When interrupt occurs, it writes the data to address= 5061H.
3. When the transmission is complete, U19 disables interrupt #1.

The transmitter begins serial transmission immediately after data is written to the transmitter

DASH #	R (LSB)	R (MSB)	MIN DATA HEX	NOMINAL HEX	MAX DATA (HEX)
001	1.00K	1.00K	13	17	1B
002	1.54K	1.00K	1C	22	27
003	2.21K	1.00K	27	2E	38
004	3.74K	1.00K	39	45	4D
005	5.11K	1.00K	4E	56	5B
006	6.65K	1.00K	5C	66	6D
007	8.45K	1.00K	6E	75	7A
008	10.0K	1.00K	7B	80	B9
009	13.7K	1.00K	8A	93	9C
010	18.7K	1.00K	9D	A6	AD
011	24.3K	1.00K	AE	B5	BD
012	35.7K	1.00K	BE	C7	CD
013	46.4K	1.00K	CE	D2	DA
014	82.5K	1.00K	DB	E3	EA
015	1.00K	1.54K		E3	
016	1.54K	1.54K		repeat	
	2.21K	1.54K		repeat	
	3.74K	1.54K		repeat	
	etc	1.54K			

Identification Resistor Values
Figure 44

port. Interrupt #1 (if enabled) occurs 520 microseconds after writing the data. When the microprocessor issues a ZVIACK cycle, the vector placed on the bus indicates that a 232TX interrupt is the highest priority interrupt pending.

(39) Identification Resistor Matrix

Each revision of the PVM circuit card assembly is assigned a unique combination of resistor values for RPVM1 and RPVM2. Two resistors are used for the PVM and the ADDA board to provide for a maximum of 196 unique revisions.

One resistor for the power supply provides for a maximum of 15 revisions. RPVM1 is the least significant digit; all possible values of RPVM1 are used for each value of RPVM2. This is demonstrated in the following list. Data values given are after correction. Correction is applied by subtracting the value read from mux channel #00, which compensates for the 'on resistance' of the mux. Refer to Figure 44.

Total number of dash numbers available is: 14 X 14 = 196.

(40) Gate Array

U19 is a custom programmed logic device. The gate array signals ZRESET and DOGSTAT tell the microprocessor that a timeout which is the result of a gate array watchdog timeout (131 millisecond) has occurred. If the microprocessor receives these signals three times in a row, the microprocessor discontinues operation and the GPWC INOP lamp is lit.

The UART for the RS232 communication signals TXD and RXD tell the gate array to enable

transmission or reception of data when one signal or the other has a high on its input. Both TXD and RXD cannot be asserted at the same time.

Address decoder signals ZVOICPR1 and ZVOICPR2 (voice EPROM enable) from the gate array tells the voice EPROMS to output aural messages.

ZMODPWR enables +5MOD for the program and data modules. When Q7 is on, +5 volts is supplied to the modules. If either of the two modules is removed from the MKVII while power is applied, the signals ZDATMODIN or ZPGMODIN goes to +5V. The gate array pins-18 and 19 (ZMMODIN and ZIDMIN) sense +5V on either line. They set the ZMODPWR line high and turn Q7 off, which removes power to the modules. Q7 and its associated parts allow the modules to be removed while the WC has power. With a low on either ZMMODIN or ZIDMIN, the gate array sends RESET signal to the microprocessors. The input prevents microprocessor operation when one or both of the modules is removed.

The gate array control decoder uses inputs listed in the following to instruct the microprocessor to perform the operations.

GATE ARRAY DECODE	MICROPROCESSOR OPERATION
ZWARMTEST	Microprocessor commences warmstart
ZRD	Microprocessor reads data
ZWR	Microprocessor writes data
ZVOICRST	Reset the voice PROMS
ZMODPWR	Module power control
ZWAIT	Microprocessor wait state
Z138A	Logic for ZMISCI signal to U34
ZNVI	Non vectored interrupt signal
ZGUIDCT	Start guidance mode (U9A to GSU)

The gate array interrupt controller signal, group interrupt, (ZGINT) sent to the microprocessor, is the OR'd output of voice chip data request (ZDRQ), receive RS232 data (RXD), and end-of-conversation from TEST CKT ADC (EOC). This signal puts a vectored address on the data bus when interrupt acknowledge is received from the status lines of the microprocessor.

Chip select is controlled by the EMD through OR gates. U25 used for isolation. Upon receipt of the signal XZRST from the power supply, NOR gate U21A deselects RAM chips U11 and U12.

(41) Keep Alive Power Supply

The +5KA power supply is held up for at least 2 seconds. This allows a write cycle initiated prior to MKVII power failure to complete. The +5KA power to the RAM is held up for at least 2 seconds after +5V is lost, so that a test for data integrity can be done to confirm the warmstart detector results. +5KA provides +5Vdc to RAM and NVM during power loss of not more than 1 minute. During normal unit operation, XZRST signal is high and Q2 is on, applying ground to the base of Q1. With Q1 on, +5Vdc from the power supply is fed through decoupling capacitors and charges up the storage capacitors. If power is interrupted, XZRST signal goes low and the storage capacitors discharge through D1 isolation diode and smoothing resistor R23. D1 and R23 ensure no current surge is allowed before Q1 can turn on. D1 also isolates +5KA from the power supply as well as other PVM circuits. +5KA also goes to the warmstart detector circuit.

(42) NonVolatile Memory (NVM)

NVM is one 8K X 8K EEPROM, U24. It is used to hold fault/status information. It also holds variable data which must be preserved during a power loss to the MKVII. The NVM is enabled through OR gate U25D. The read/ write function is controlled from the gate array. ZRD is inverted by U16F, NANDed by U15D for isolation, and tied to XZRST through R55. This allows active low XZRST to act as chip select ($\overline{OE}$) to ensure NVM write cycle completes if a power loss occurs in mid cycle. If the write cycle is already in process when a power loss occurs, U24 freezes input data when $\overline{OE}$ is asserted. Internally the NVM continues and finishes the write cycle. +5KA ensures that the write cycle completes. If $\overline{OE}$ and write enable (WE) go low simultaneously, NVM goes to a lockout state and prevents the write operation. At the same time, NVM allows the present write cycle to complete.

(43) Dual Port RAM

U37 is the master and U36 is the slave of the dual port RAM circuit. Two 4K X 8 RAM are used by the ADDA and the PVM subassemblies to pass data and status information to each other. The PVM also sends commands to the ADDA through the DPR. The PVM commands the read/write operations. EMD provides DPR chip enable signals. ZDPRAMBSY signal is used by the gate array to tell the microprocessor the status of the DPR to ensure that the DPR completes its processing activities before more data, status, or commands can be passed between the ADDA and the PVM.

(44) Warm Start Detector

The warmstart detector informs the microprocessor, through the miscellaneous input buffer U34, if the microprocessor needs to perform a warmstart (power off less than 0.8 seconds) or a coldstart (power off more than 1 second). A warmstart signal is also sent to the ADDA through J9 pin-12 to inform the ADDA microprocessor. During normal operation, ZWR and D0 lines are set high, setting U13A. Q goes low and turns on Q23. Voltage from the +5KA circuit charges C101. This input to comparator AR10 causes AR10 output to be high. A high on U13B indicates to the gate array a warmstart instead of a coldstart.

If power is lost, XZRST goes low and resets U13A which in turn shuts off Q23. C101 discharges through R117 (1 second time constant). XZRST sets U5D to the open collector state and is then inverted by U21D which puts a low to the clock input of U13B. At power restore, XZRST goes high, qualifies U5D, output of U5D goes low, is inverted by U21D to a high. This rising edge of the change is detected by U13B as a clock pulse. U13B then clocks in the output of AR1A. If the warmstart line is high, the microprocessor samples the data lines on the miscellaneous buffer if the ZRESET line is asserted. If the microprocessor detects a warmstart condition, the list of start up tests is abbreviated compared to a coldstart operation.

The microprocessor then resets the warmstart detector. The signal ZWARMTEST from the gate array is used to test the detector. It is purposely set to give a warmstart indication to check warmstart operation.

(45) Miscellaneous Microprocessor Port

The following circuits provide status to the microprocessor:

```
Warmstart Detector
Voice Test Monitors
Guidance Watchdog Timer
Gate Array Watchdog Timer
```

ADI flag outputs to GSU

All the tests are enabled by the signal ZMISCI from the EMD.

(46) Lamp Port

U22 and U23 output discrete signals to control warning/status lamps. The outputs are controlled by DISCOLAT signal from the gate array. U22 is reset with a low ZRESET sent from the gate array.

U23 is reset through AND gate U26B. ZRESET is normal high, and guidance validity output from guidance watchdog timer (GUIVAL) is high when guidance processing is normal and valid. If either ZRESET is enabled low or GUIDVAL goes low, a clear (low) is sent to pin-1 of U23. This disables MKVII guidance deselect RSTSEL signal, and removes MKVII ADI flag outputs PVMFLAG1 and PVMFLAG2 through AND gates U26A and U26C. These signals remove the following command signals: flight director lamps, speed command approach (SPD), speed command take-off (T/O) speed, and Traffic Alert Collision Avoidance System (TCAS) inhibit.

(47) Voice Circuits

The voice circuits of the WC contain the MKVII interface to the host aircraft cockpit speaker and interphone systems. The voice circuits issue the audio alerts to the pilots using the following software steps:

1) Software resets the voice chip prior to issuing a message, and at the end of a message.
2) Software enables the voice chip prior to issuing a message.
3) Software selects the audio level output.
4) Software identifies the voice message number to be announced.
5) The voice issues an interrupt to indicate that a message has been completed.

The voice circuitry consists of the voice chip to synthesize words, 2 voice PROMs which contain voice messages, a programmable gain amplifier for volume control, 8-ohm and 600-ohm audio outputs, mute circuit, test monitor circuit to ensure proper operation and a constant current source for the speakers.

The MKVII audio circuits support four program pin selectable audio levels. The power output levels are 1/4 watt, 1/2 watt, 1 watt, and 2 watts. The nominal level is 1 watt. The standard audio output levels can be changed to produce twice the output power or 1/2 the output power by the use of two program pins. The 'all modes inhibit' input discretes turn off the audio portion of any alert/warning.

(48) Voice Chip

U30 synthesizes the voice messages. It communicates with the voice PROMs over a 17-bit address bus and an 8-bit data bus. ALE signal from U30 controls the address latch U33.

(49) Voice Circuit Input Signals

Signals I0 through I7 (8 bits on the PVM data bus) carry the message number to U30 to specify which message is to be processed. Up to 256 messages can be specified (in binary code). The control lines are discussed in the following paragraphs.

$\overline{ST}$ (signal ZWR from the gate array) starts the voice synthesis.

$\overline{CS}$ ZVOICE (from EMD) is the chip select.

$\overline{BSY}$ (ZVOICBSY 1 wait state) is sent to the gate array indicating voice synthesis is in process. This causes the gate array to send ZWAIT to the microprocessor.

$\overline{RST}$ (ZVOIRST) from the gate array resets U30 and the voice test monitor circuits.

$\overline{DRQ}$ (ZDRQ) is sent to the gate array to combine with D8 (bit 9) to enable the proper voice PROM.

AVO synthesized audio output ANAVOI is sent to the program gain amplifier to set the level of audio sent to the speaker.

Address lines A0 through A8 is 9-bit address bus for the voice PROMS.

Address lines ASD0 through ASD7 mux 8-bit address out to the voice PROM and 8-bit data in from the voice PROM.

X1 and X2 are input signals for the 640 kHz oscillator used in voice synthesis.

REF signal input to U30 provides current source from AR3A and AR3B. This current source ensures constant audio level output.

(50) Voice Chips

U32 is PROM 0 and U31 is PROM 1. These PROMs hold voice message information for the voice chip. U32 holds lower order group messages and is controlled by ZVOICPR1 from the gate array. U31 holds upper order group messages and is controlled by ZVOICPR2 from the gate array.

(51) Voice Chip Operation

The extended memory decoder selects the voice chip by asserting ZVOICE and gate array signal ZVOIRST which clears the voice chip. When the microprocessor puts the message number on the data bus, the gate array strobes the message number into the voice chip at the same time the gate array asserts ZWR. Once the message number is latched into the voice chip, the data lines can be disabled and the voice chip addresses and sends the data to the voice PROMs. U30 sends ZDRQ to be ANDed in the gate array with D8 to set the proper PROM enable. Depending on what the message is that has been selected, ZVOICPR1 selects U32 and ZVOICPR2 selects U31. U30 sets ZVOIBSY and addresses the correct PROM for the desired message. The PROM responds to the voice chip with the message address. U30 readdresses the PROM and reads the message data. The message is synthesized in U30 and output as ANAVOI to the programmable gain amplifier U29. When the message synthesis is complete, ZVOIBSY is cancelled.

(52) Programmable Gain Amplifier

Programmable Gain Amplifier, U29, is a multiplying DAC chip. Input from the voice chip, ANAVOI, goes to U29 pin-19 VRef input. C13 removes +4Vdc (the DC level the audio signal is piggybacked with) making the input to pin-19 1Vpp ±0.5Vdc. U29 is programmed with a gain from 0 to 1. ZLOUDDA from the EMD latches data lines D0 through D7 into U29 to set the gain. 11111111 =256= gain of 1. 00000000=0=gain of 0. The output to AR7D is

ANAVOI X 0-1. The output of AR7D is feedback to U29 RFB by voltage divider R92 and R93. This input to RFB changes the gain output to 0 - 19.2. The output from the amplifier goes through a 3-pole high pass filter and a 3-pole low pass filter to remove digital noise from the audio portion of the signal. The signal is then fed to the 600-ohm audio amplifier and the 8-ohm amplifier.

(53) 600-Ohm Audio Amplifier

The output of the low pass filter is coupled to the input of AR7B by C86 and R106. The audio signal is then inverted and sent to pin-1 of T1. This audio signal is also sent to the + input of AR7C and then to pin-3 of transformer T1. The audio message is coupled across T1 to the input of the Voice Test Monitor circuit through MON600H. This circuit is used to detect a shorted output. U8A diode array clamps the audio signal to prevent any voltage spikes from being sent to the 600-ohm headphones. If a short is detected, no output is sent to the monitor circuit.

(54) 8-Ohm Audio Amplifier

The audio output of the low pass filter is coupled across R84 to the input of AR8. This audio input drives operational amplifier AR8 to draw current through ±14Vdc. Positive (+) voltage is developed across R90 and R91. Negative (-) voltage is developed across R88 and R89. Q20 and Q21 are 180^{o} phase shifted from the input of the audio acting as a push pull circuit. Audio is developed across R70 to the 8-ohm audio output. MON8L and MON8H are also sent to the voice monitor test circuit. R70 is the sensing resistor for detecting over-current condition.

If a speaker develops a shorted output, the current draw increases and voltage is developed across R70. Q19 and Q22 turn on and Q20 and Q21 are clamped to ±14Vdc. This decreases the output across R70 and turns off Q19 and Q22. The output to the speakers increases and the cycle of clamping the output continues until the short is removed.

(55) Mute Circuit

The mute circuit is designed to prevent 'popping sounds' in speakers when power is applied or removed. When power is first applied to the unit, field effect transistor (FET) Q24 is self-biased on, and any audio noise on the output of the low pass filter is shunted to ground. R120 and C102 provide a delay of 10 milliseconds. When -V is sufficient to shut off Q24, the audio is available to the 600 and 8-ohm amplifiers. On power down, Q25 is turned on by XPINT conducting the output from the high and low pass filters to ground. The programmable gain amplifier is set to default to a gain of 0, making the output of the high and low pass filters negligible. 10 milliseconds after power down, Q24 is biased to turn on at the next power up and provides mute protection for the circuit.

(56) Voice Test Monitors

This circuit ensures that the voice and audio amplifiers are operating properly. Every 3 seconds, a low level audio click is sent to the 600 and 8-ohm audio amplifiers. That output plus any message audio output is monitored. The click is inaudible to the pilots. MON600H is developed across R110A/B and input to AR9C. U8A/B is used to shunt high voltage spikes to ground. When the audio amplifiers and the voice circuit are active, AR9C output toggles. This toggle acts as the clock input to U20A (D type flip/flop) and continuously sets U20A. Q goes low to send Z600VAL signal to the miscellaneous input buffer, U34, and is then read by the microprocessor from the data bus to the address inputs on the microprocessor.

microprocessor.

ZVOIRST is used by the gate array to reset the voice chip. It also resets U20A/B.

MON8H and MON8L are sent to AR7A, amplified and sent to AR9D. If the 8-ohm circuit is working, the output of AR9D toggles and sets U20B, Q goes low, and the Z8VAL is read by the miscellaneous input buffer and by the microprocessor.

(57) Flight Director Lamp Drivers

There are 11 lamp driver circuits:

```
4 GPWC lamp drivers
4 Windshear lamp drivers
3 Flight director lamp drivers
```

The flight director lamp driver that provides TCAS signal is used by the MKVII to inhibit the TCAS during any aural message.

All lamp drivers work by applying a ground (current sink) as an output.

(58) GPWC Lamp Driver

Signal GPWDISCO (active high) from the microprocessor through the lamp port is inverted by U16B to a low and is applied to U10B (open collector NAND) with the output acting as an open. AR5A receives a small bias on its + input (+0.17 to 0.2Vdc) from the voltage divider R59 and R68. This signal is known as VREFCM and it drives AR5A output to turn on Q3, which provides ground to GPW +28Vdc lamp. Diodes D8 through D10 isolate the output of Q3 for one of three possible lamp lines.

NOTE: *The purpose of three lamp lines is to make interfacing with a variety of aircraft wiring schemes. Only one lamp for the GPWC is connected in each aircraft.*

If an over-current condition exists, voltage is developed across sensing resistor R29. If that voltage becomes more positive than VREFCM bias to AR5A, the output goes low and turns off Q3. When the voltage across R29 becomes less than VREFCM, AR5A goes high, Q3 turns on and the cycle starts again allowing the lamp to provide warning, even with too much current draw in the lamp circuit. In this situation the lamp flickers but continues to provide warning responses.

Diode U14D shunts positive spikes to VR1 (82Vdc zener). VR1 shunts high voltage spikes to ground. U14D also isolates other lines from other lamp driver voltage shunts. VR1 shunt goes to the other drivers as DIODECM. MOSFETs have an internal parasitic diode to shunt negative spikes.

(59) GPWC Inoperative (INOP) Lamp

The lamp is self biased to light with no MKVII power. This provision alerts the pilots that the WC is not operational. Power comes from the aircraft and the lamp ground comes from the MKVII. The lamp brightness is reduced in this circumstance.

ZINOPDISCO signal from the microprocessor through the lamp port at logic high turns on Q14. Diode D7 is forward biased due to Q14 applied ground. +12Vdc is dropped across R53. Ground applied to the gate of Q18 shuts it off. No lamp output is the result.

If the GPWC becomes inoperative and power is supplied from the MKVII, ZINOPDISCO is

a logic low that turns off Q14. +12Vdc is coupled to the gate of Q18 through D7. With Q18 on, ground to the lamp is supplied and the lamp lights. If an over-current event occurs, voltage developed across R66 turns on Q15. Q15 applies ground to Q18 gate turning off Q18.

If a no power to the MKVII situation exists, +28Vdc supplied directly from the aircraft power supply is coupled to the gate of Q18 through R62. This biases Q18 on about half as much as a normal. The INOP lamp receives half as much current as usual so the INOP lamp is lit but is dimmed.

(60) Windshear Guidance Recovery Circuit

This circuit consists of a 12-bit DAC, 3 pairs of operational amplifier drivers, a guidance watchdog timer, and a start circuit.

U18, the DAC, contains 4 separate 12-bit DACs. Three are used and are bipolar. The remaining DAC is not used. All control signals for the guidance operation come from the gate array. +5VREF provides voltage reference for the DAC from U7.

ZGUIDAT selects the correct DACs using address bits A1 and A2. ZGUIDAT latches data on the data bus (D0 through D11) that is to be converted.

When ZWR is low (after ZGUIDAT is low and ZGUIDAT goes high), DACs can output the analog data. If ZWR goes low after ZGUIDAT is low, and then goes high before ZGUIDAT, data is input and is ready to be output but the analog output does not change.

ZRD allows read back of output for data and error checks performed by the microprocessor.

ZRESET from the gate array provides a reset to the circuit.

D0 through D11 provide the 12 bits of input from the data bus. Each of the three DACs handles a specific group of commands.

```
DAC A is used for pitch commands.
DAC B is used for roll commands.
DAC C is used for fast/slow commands.
```

Pitch commands are digitized by U18 (address 00) and the analog output is sent to AR1A/AR2A through R7 and R9. Outputs are inverted and doubled and sent to the GSU through the backplane J2 connector. U4 is used as a spike protector.

R19 provides feedback to AR1 and AR2 to be based on the ADI load. With R19 in the circuit, constant feedback is assured. For output checks and comparison, the outputs of the operational amplifiers AR1 and AR2 are fed back to the configuration/test interface circuit.

(61) Guidance Start Circuit

ZGUIDCTL from the gate array sets U9A when data line D2 goes high. The Q output goes low and is then inverted by U28F to a high. This is fed to the GSU (a +5Vdc 100 - 200 millisecond pulse) to cause the GSU to take over the guidance indication function for GSU #1 (Captain). GSU #2 (First Officer) is controlled by lamp port data bit 11 (U23 pin-9).

NOTE: *U9A is cleared by the output of the guidance watchdog circuit. It is active low and gives the watchdog (WD) timeout.*

(62) Guidance Watchdog Circuit

This circuit is used to ensure timely updating of the guidance processing.

ZGUIDMON from the gate array transitions high to low to high. With a logic high on data line D3, this sets U9B (half of D type flip/flop). The O output transitions from low to high and triggers U17A (half of dual monostable multivibrator). An input to U17A is tied to ground and C input is tied high (+5Vdc from pullup resistor R22D as the GSU monitor circuit is not used). This causes U17A to trigger the Q output to go low for 123 millisecond (time constant determined by R44 and C43). This disqualifies U45A, not AND (NAND), and the output GUIVAL goes high and also clears the input to the guidance start circuit. Input U45A is ZRSTDISABLE, a +5Vdc signal from pullup resistor R68I at the gate array.

If the guidance watchdog is not retriggered by data line D3 being high and ZGUIDMON transitioning within 123 milliseconds, and U17A times out, Q output goes high, qualifies U45A, then Q goes low. U9A is reset and GUIVAL goes low, indicating an invalid guidance processing. GUIVAL goes to the miscellaneous input buffer. The guidance watchdog timer is reset with ZRESET sent from the gate array.

NOTE: Software is designed to reset the guidance WD timer every 100 milliseconds. The timer is used to ensure the software for guidance functions properly.

(63) Configuration/Test Interface

Configuration/test interface is used to check configuration of the WC boards by reading configuration resistor values on the ADDA, PVM, and power supply boards. This ensures that properly configured boards are used with the correct software version.

RPOWER is the configuration resistor value from the power supply. It comes into the PVM through J4 pin-7 and from there goes to U1 pin-5 of the PVM ohmmeter circuit. RADDA1 and RADDA2 are the ADDA configuration values and go to J8 pins-1 and 2 on the PVM, then to U1 pins-6 and 7. R48 and R49 are the PVM configuration resistors and are input to U1 pins 11 and 12.

Guidance outputs, pitch, roll, fast/slow, and GSU validity are also processed using the ohmmeter circuit. Inputs are digitized by U2 and sent to the microprocessor for processing. U3 multiplexer switches guidance validity and feedback on AR6D pin 14 to multiplexer U1 pin-10 through the level shifter circuit.

Data lines D0 through D7 (D0 - D7) are input to U35 where they control the channel selection of mux U1 and U3. Only D0 - D5 are used. ZMUXALE from EMD and ZWR from the gate array are NANDed in U25A. If both are true (low), the output goes low and is inverted by U6E, and that logic high enables U35. D0 - D5 is output as MA0 - MA5. MA0 - MA2 control channel selection for mux U1, mux U3 uses MA3 - MA5.

The configuration ohms values are input to mux U1. Output of U1 is applied to U2, ADC. U7 is a precision +5V reference. The output of U7 is also used as reference for U18 DAC. U2 ADC through isolation buffer AR1D is used with R3, a 10K precision resistor connected to the output of U1 as a reference in verifying configuration correctness. R3, +5Vdc reference, and the configuration ohms value form an ohmmeter circuit to check configuration values using Ohms Law (Voltage = current X resistance).

The output of U1 is fed to U2, an 8-bit DAC. The clock input is a 666.7 kHz developed by R1 and C1 time constant. Voltage reference is supplied from U7 through AR1D. +V from U1 and -V are ground. U2 is selected by ZRIDAD from the EMD. ZWR from the gate array is

ANDed with ZRIDAD (100 milliseconds later) and U2 starts the conversion. When complete, U2 sets INTR low. This is inverted by NAND U45B and sent as end of conversation (EOC) to the gate array. The gate array unasserts ZWR and asserts ZRD, and the digitized data is placed on the data bus as D0 - D7.

Multiplexer U3 inputs guidance outputs and GSU validity signals. The mux is controlled by MA3 - MA5. Output of the mux is sent to AR6D. AR6D is a level shifter with a gain of 0.5, with +1.67Vdc applied to the + input through voltage divider R73 and R74. This allows ±5Vdc from the guidance outputs to be shifted to 0 - +5Vdc. The output of the level shifter is sent to input of mux U1.

NOTE: GSU validities are input to U3 and GSU status monitor AR9B. The software performs the monitor functions. This is because of a variety of validity levels from the aircreft.

The output of AR9B is signal SWUMON and is sent to guidance watchdog monostable multivibrator U17A. It is tied to +5Vdc through pull-up resistor R22D.

(64) RS232 Interface

The RS232 bus allows the PVM to communicate with the MKVII ATE. The receiver circuit includes VR2, a 4.7Vdc zener, and inverter U5F. The input is sent to the UART of the gate array as RXD.

Transmit circuit includes output from the gate array UART TXD. It is sent to AR6C, inverted and the output is sent out of the WC as 232TX through the backplane connector.

E. Power Supply Board

The MKVII power supply input is 115Vac, 400 Hz at J6 from the aircraft. Input to T1, pins-1 and 2, is split by the three separate windings to produce ±24Vdc, ±14Vdc, and 42Vac. Figure 45 shows the block diagram of the power supply.

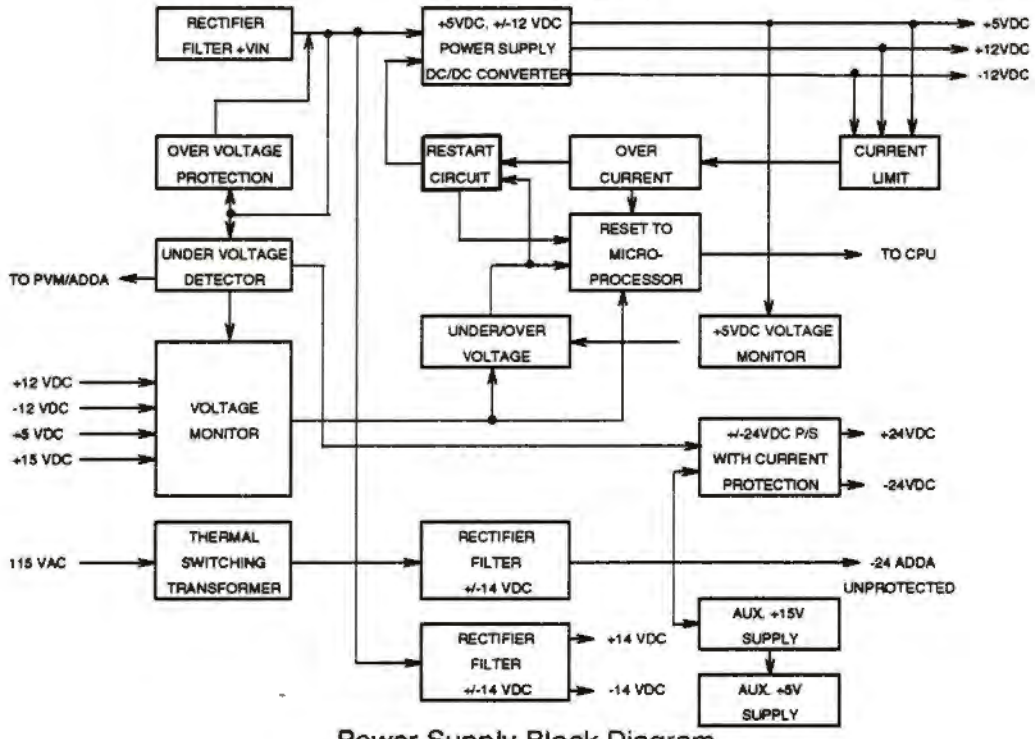
The MKVII power supply provides power to the ADDA and PVM boards supplying ±14Vdc, ±12Vdc, and +5Vdc. ±24Vdc developed in the MKVII power supply is used to power 2 external sensors.

Whenever the power is first applied to the WC, both microprocessors in the MKVII receive a reset. A hardware latch, warmstart, on the PVM is set to indicate if the power has been off less than 1 second. If power to the MKVII is off longer than 1 second, the hardware latch indicates a coldstart for the unit is necessary and a different startup routine is performed in the MKVII software.

The power supply generates an NMI when the voltage output drops below a certain level. This NMI is sent to the microprocessor on the ADDA and PVM boards to reset them. The voltage level the NMI (XPINT) is designed to give the microprocessors enough time to finish and store information needed to restart the MKVII processes. The software response to this NMI is to save the current state of the software. When the proper level of power is restored, the WC uses the shutdown information stored by the ADDA and PVM microprocessors to resume operation, and automatic BIT testing to take up where it is most appropriate in time.

With this capability of the ADDA and PVM microprocessors to 'remember' where they were in the software processing at the time of power loss, the WC resumes software processing in a routine best suited to the circumstance (warmstart or coldstart). Resumption of the WC operation is much faster for a warmstart using this scheme.

T1 couples input and provides isolation for the AC from unwanted DC voltages.



Power Supply Block Diagram
Figure 45

±14Vdc is used by the PVM to power the 8-ohm audio circuits. ±14Vdc is rectified by D13 and filtered by C37 through C39.

±24Vdc is used to power the mini air-data computer and the biaxial accelerometer. This power circuit input is full-wave rectified by D12 and filtered by C28, C31, C41, and C42. ±24Vdc is used by the current limit circuit, ±15Vdc, and ±5Vdc auxiliary supplies.

(1) Auxiliary Supplies

VR16 is a 3-terminal adjustable voltage regulator. An input of +24Vdc produces +15Vdc output filtered by C35. The +15Vdc output is used as an internal power supply reference voltage.

The output from the ±24Vdc auxiliary supply is input to VR15, the +5Vdc auxiliary power supply. VR15 is a linear +5Vdc voltage regulator and is used as an internal +5Vdc power supply reference (+5C). The output is filtered by C32.

(2) ±24Vdc Current Limit

±24Vdc are two separate, +24Vdc and -24Vdc current limit circuits. For the purpose of the manual, only the +24Vdc current limit circuit is described. The -24Vdc current limit circuit performs in an identical way as the +24Vdc.

The +24Vdc output from D12 voltage rectifier is connected to the emitter of Q13 and source of Q11. Q13 is off and Q11 is on. The gate of Q13 is limited to 10Vdc by VR11. In this circumstance, the drain of Q13 is +24Vdc, indicating no over-current condition exists.

(3) Current Limit Circuit

If an over-current condition is created because of a short externally to the +24Vdc circuit, voltage is coupled to the base of Q13 by the resistors R76, R73, and then O13 turns on. Current flows through R111 and R110 through Q13. Voltage drop on R111 (+3.6Vdc) turns on Q17. C29 discharges through R82 and +V is developed to feed AR4D pin-13. This is compared with +12Vdc reference AR4D12. The bias is set by R84 and R99. After 40 to 45 milliseconds, the voltage on R82 drops below +12Vdc and ARD14 output is high.

(4) One-Shot Circuit

ARD14 high output (during external Power Supply short) turns on Q16. With Q16 on, C34 discharges through R88 (47 microseconds). Voltage developed by R88 and C34 is input to AR4 pin-9 to compare with +18.9Vdc on AR4 pin-10. If the voltage on R88 is below the threshold, AR4C pin-8 goes high. This high level goes to Q11 gate and turns Q11 off. With no voltage or current flow from Q11, Q13 turns off.

The following over-current example requires several conditions:

```
Q11 is off, AR4C pin-8 is high, and C34 has no charge.
Q13 is off.
The bias set up by R73 and R76 has no current flow.
Q17 is off, and no current flows through Q13.
```

C29 starts charging, with a time constant of 54 milliseconds, through R82 and R98. At about 45 milliseconds, C29 reaches > +12Vdc and overcomes the +12Vdc reference. AR4C pin-9 goes low.

With Q16 turned off, C34 starts to charge through R88 and R87 (time constant = 150 millisecond). C29 takes 255 milliseconds to charge up to +18.9Vdc. C34 charges to AR4C pin-9 and overcomes the +18.9Vdc reference AR4C. The output AR4C pin-8 goes low. Q11 is now on and the cycle starts over with the following time frame:

Short occurs:

```
Circuit is on for 45 milliseconds
Circuit is off for 300  milliseconds
Circuit is on for 45 milliseconds
Circuit is off for 300 milliseconds
```

With Q14 turned on, C34 discharges, performing the same function as Q16, and is controlled by the signal - LPWR from the GPWC power circuit. If the input voltage is less than 37Vdc, - LPWR goes low and turns on Q14. C34 discharges and 80 microseconds later AR4C output goes high and Q11 turns off. No ±24Vdc is output to the WC external sensors.

(5) +42Vac

D14 rectifies +42Vac from the secondary winding of T1. C9 and C43 through C45, filter the +42Vdc and provide a 10-milliseconds delay to protect WC circuits from a voltage surge at power up.

Input over-voltage protection is provided by Q4, Q5, VR4, VR5, VR6, and R10. If the input voltage is greater than +62Vdc, VR6 conducts and voltage is dropped across R13 equal to about +21.5Vdc. Q5 is on and shunts the input voltage to the gate of Q4, maintaining a

0.2Vdc difference of potential between Q4 gate and source, causing Q4 to be off.

The input voltage across R10 attenuates the voltage to protect VR4 from power levels above its 600W rating. VR4 is a transorb diode designed to shunt the excessive voltage to ground.

The input +42Vdc to U1, DC to DC converter, is pin-4. Ground is pin-3. Three DC voltage values are output. Pin 7 outputs +5Vdc, pin-6 is ground, pin-8 is +12Vdc, and pin-5 is -12Vdc output.

(6) Under Voltage Detector

The input voltage is coupled into the under voltage detector circuit. This circuit is designed to detect and warn the WC microprocessors of any low voltage condition. The XPINT signal from the power supply, informs the microprocessors of imminent power down due to input voltage of less than 39V. XZRST from the power supply resets the ADDA and PVM microprocessors.

AR1B is a 'less than 39Vdc' comparator. AR1B pin-6 is the reference input and is a +6.2Vdc potential fed by VR7. With 42V input to the voltage divider R15 and R16, input to AR1B pin-5 is 6.6Vdc. AR1B output is high shutting Q7 off. If the 42Vdc drops below 39Vdc, AR1B pin-7 goes low and turns on Q7, sending XPINT to ADDA microprocessor directly to pin-46, NMI. By providing NMI at 39Vdc, the PVM microprocessor has time to store processing information in NVM.

AR1A is a 'less than 37Vdc' comparator. Q6 collector varies +VIN depending on +42Vdc input. The emitter of Q6 supplies AR1A a constant +14.3 voltage.

VR7 provides a +6.2Vdc reference to AR1A pin-2. Voltage divider network, R18 and R19, gives +7Vdc at AR1A pin-3. If the input voltage on pin-2 drops below +37Vdc, AR1A pin-3 drops to +6.1Vdc, causing the output of AR1A pin-1 to go low. A low output of AR1A turns on Q9 which in turn applies ground to send a reset signal to the PVM gate array. By having low voltage detection for +39Vdc and +37Vdc, the warning computer microprocessors have multiple machine cycles to store processing information before the unit is reset or shut off.

Line sense on U4 of the voltage monitor circuit also receives output from Q9. A ground at Q9 is also sent to ±24Vdc Current Monitor circuit one shot transistors, Q14 and Q15. These transistors control turning off the ±24Vdc of the MKVII.

(7) +5Vdc and ±12Vdc Output With Current Limit

The U1 output to the power supply is +5Vdc and ±12Vdc. +5Vdc output from U1, DC to DC converter, develops across current sensing resistors R4 and R5 and on to +5Vdc distribution. AR3B pin-6 is biased at 4.9Vdc and AR3B pin-7 must be greater than AR3B pin-6. If an over-current condition develops, more voltage drops across R4 and R5 and this causes the voltage difference between AR3B pins-6 and 7 to leave pin-7 less positive than pin-6. When pin-6 is more positive, the output of AR3B goes low, producing a low output from AR3A pin-2, which sends a control signal to U2A. U2A is a monostable vibrator with a time constant of 110 to 150 milliseconds set by R43 an C17.

Output from AR3C pin-14 turns on Q8 which controls the output of the DC to DC converter U1. U1 output is off for the duration of the time constant of U2A. D11 provides +2.5Vdc reference to reset the output of AR3B to a logic high at power recovery. D11 is normally back biased by +5Vdc on AR3B pin-7.

Q2 and Q3 provide over-current detection for +12Vdc. R6 and R7 bias Q2 on if an over-current condition exists. With Q2 and Q3 conducting, ground is applied to the input of AR3A pin-5.

-12Vdc uses Q1, Q2, and Q3 for over-current protection. R3 is a current-sense resistor used to bias Q1 on in an over-current condition. With Q1 turned on, Q2 and Q3 turn on, applying a ground to the input of AR3A.

(8) Restart Circuit

The Restart circuit turns off the +5Vdc and ±12Vdc for 150 milliseconds during the over-current condition. At the end of the 150 milliseconds, U1 is reset to output voltage. AR3A is used as a buffer/comparator for the Restart circuit. A +2.5Vdc Vref is applied to AR3A pin-4. The + input of AR3A pin-5 is +5Vdc. The +5Vdc goes low in an over-current condition from either the +5Vdc or the ±12Vdc.

C25 and R62 provide a 5-millisecond delay before the output of AR3A goes low to prevent momentary power surge from disabling the Power Supply. If pin-2 of AR3A goes low, a reset is applied to the input of U2A. U2A is a monostable multivibrator with a pulse time of 150 milliseconds (set by R43 and C17). With a low output from pin-4 of U2A to pin-9 input of AR3C, pin-14 of AR3C at that time goes low for 150 milliseconds. That low signal is applied to the cathode of Q8 turning on the opto-isolator. With Q8 on, U1 the DC to DC converter output, is off for 150 milliseconds. Ground is applied to pin-1 from pin-3.

When U2A times out, the reset circuit sets U1 to output its voltages again. If an over-current condition still exists, the cycle starts over. Additionally, when an over-current event occurs, a reset to the PVM microprocessor is sent with the signal XZRST by way of U3C pin-9 receiving a low on its input.

(9) Voltage Monitors

U4 is used as a voltage monitor for the ±12Vdc, +15C, and +5C circuits. The ±12Vdc and +15C input lines use sensing resistors and voltage divider networks to condition the input to 2.5Vdc to be compared with VREF. Pin 3 is the 2.5Vdc reference output used by the different voltage levels for this voltage monitor. Pin 1 of U4 uses R40 to set the basic tolerance the device uses in monitoring.

Pins 11, 12, 13, and 14 are the sense inputs for the 4 voltages being monitored. Pin 15 is an inverted input to monitor the -12Vdc. C16 provides a 0.25 millisecond delay for fault reporting which prevents nuisance faults. Pin-9 reports over voltage and pin-10 reports under voltage conditions to produce the signal XZRST.

Pins 5, and 7 comprise a line sense. Pin 5 is the signal input, and pin-7 the output. A low output on pin-7 indicates a low voltage condition in the less than 37V circuit and is used as an additional monitor. From this circuit, XZREST is sent to the microprocessors. Both over/under voltage detection circuits produce a low (or ground) to the input of U2B which produces a signal to Q8 to inhibit U1 outputs.

(10) +5Vdc Monitor Circuit

Additional monitoring ensures that the +5Vdc produced by U1 is between +4.78Vdc and +5.22Vdc. AR2B is designed to detect voltage below 4.78Vdc, and AR2A detects voltage above 5.22Vdc. If the +5Vdc drops below 4.78Vdc, AR2B output goes low sending a low input to U2B. If the +5Vdc goes above +5.22Vdc, AR2A sends a low input to U2B. By

fully monitoring the +5Vdc and providing 40 to 50 milliseconds delay (using R55 and C54, in reporting the over or under voltage if such is detected), the power supply has time to correct the problem if it is caused by a momentary transient. This prevents the WC from producing an unnecessary microprocessor reset for power failures or faults.

(11) Schmitt Trigger

U3, a quad NAND Schmitt trigger, and Q10, a PNP transistor, send the XZRST signal. NAND gate U3 takes input level information from +5Vdc, ±12Vdc, +5C, and +15C circuits, allowing each circuit to trigger XZRST if a fault occurs. A high output on pin-3 of U3A turns off Q10 allowing ground to be sensed through R51 sending XZSRST to the WC microprocessors. Input delay circuit, C24, R55, and R56, develops a 40 to 51 milliseconds delay to keep the input to U3D pin-13 low keeping XZRST low while the Power Supply voltages settle. A low input to U3C or U3D provides a high output which is inverted by U3A and U3B and then is applied to the base of Q10. A high on the base of Q10 turns it off. With no current flow, ground is sensed as XZRST through R51.

NOTE: Any value of resistance of 4.7K or less is seen as ground by CMOS devices.

D15 isolates the output of U3C and U3D. If no fault occurs in the power supply, the output of U3C and U3D is low, Q10 is biased on, and +5Vdc is developed across R51, keeping XZRST high.

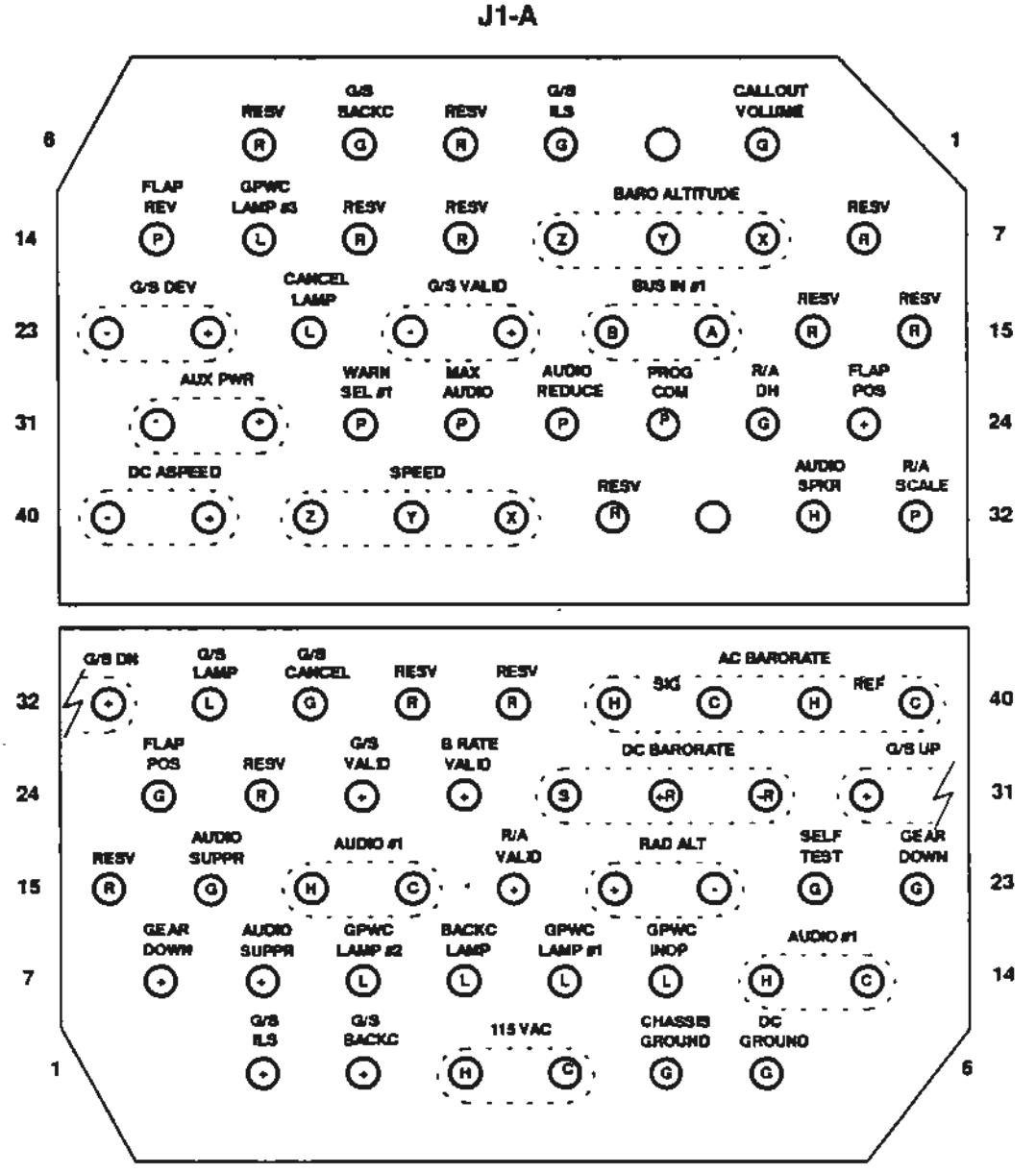
F. **Backplane Connectors**

On the MKVII rear panel, the connectors J1 through J6 provide the input/output interface between the aircraft. Figure 46 shows the pin-outs for the backplane.

G. **EMI Filter**

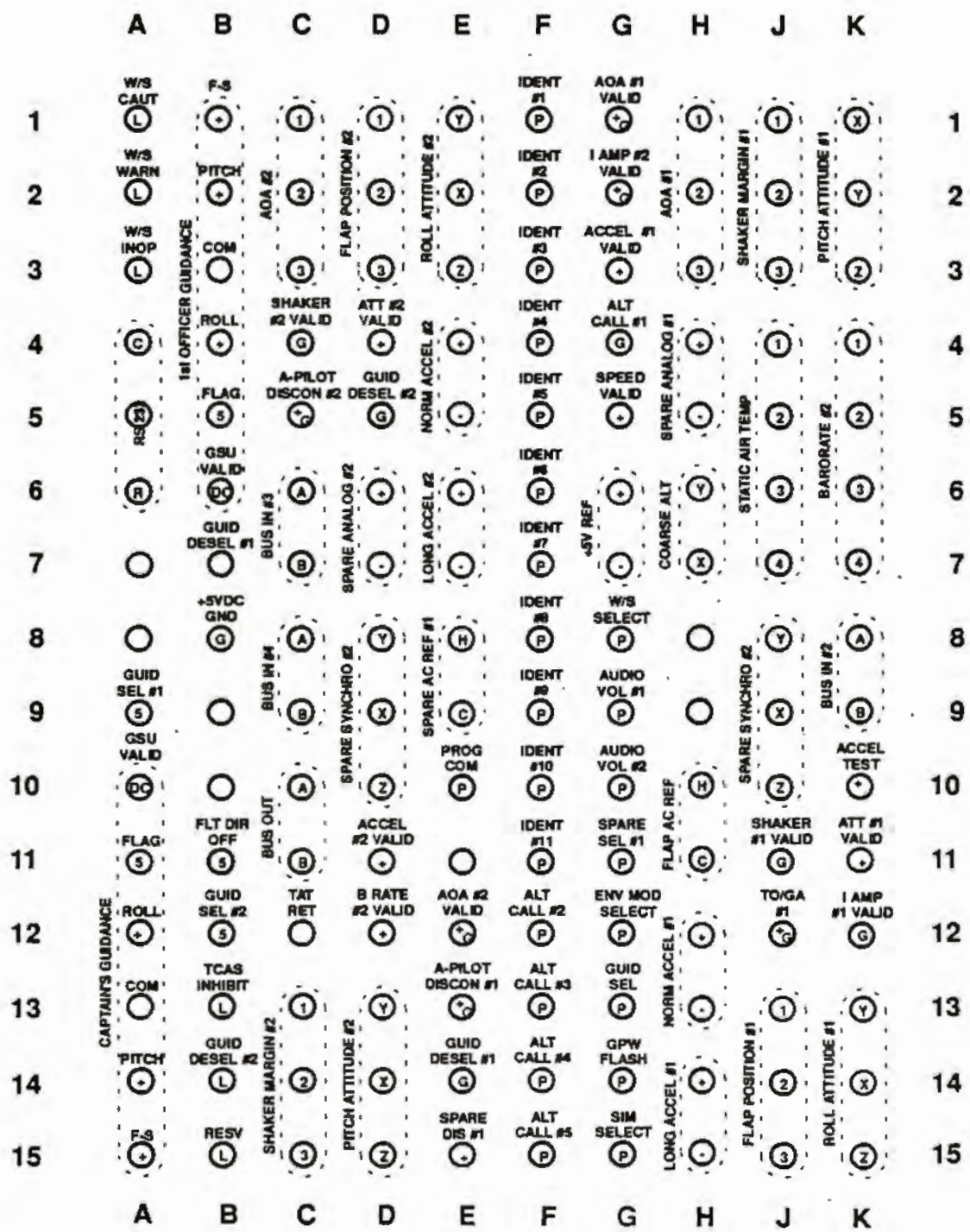
The EMI filter provides protection to the MKVII from power spikes that can be generated in the aircraft power plant. The EMI Filter is a series-pass protection circuit, filtering voltage spikes with inductors and capacitors. F1 and F2 provide fuse protection to prevent voltage spikes exceeding 125Vac from reaching the MKVII signal processing boards.

Lower Connector - J1



Backplane Pin-Outs
Figure 46 (Sheet 1)

Upper Connector - J2



Backplane Pin-Outs
Figure 46 (Sheet 2)

TESTING AND TROUBLESHOOTING

1. General

This section of the manual provides a description of the acceptance test procedure (ATP), troubleshooting techniques, and schematics necessary to test and troubleshoot the warning computer system (MKVII). The MKVII has many built-in-tests (BIT) to alert pilots of ground proximity warning system (GPWS) problems and to direct repair technicians in troubleshooting failures. The troubleshooting information relates to the unit under test (UUT) in the repair shop.

2. Skill Level of Repair Technicians

A repair technician must have the following education and experience to be effective in troubleshooting the MKVII:

AA or equivalent degree in electronics.
Extensive knowledge in microprocessors.
Extensive knowledge in digital and analog circuits.
Some experience using a personal computer (PC).

3. Test Equipment

The MKVII WC ground support equipment (GSE) (P/N 951-6517-003, -004, or -005) is used to test the MKVII UUT in conjunction with an IBM-compatible PC. The MKVII WC GSE (tester) provides stimulus to the UUT and measures and records the response of the UUT. A list of test equipment and original equipment manufacturer (OEM) information is included in Figure 101. (Refer to the GSE Hardware User's Guide, Document 951-6517-603, for more information on the MKVII test equipment.)

NOTE: Test equipment substitutions are permissible if substituted equipment has equal or better performance characteristics.

Figure 102 shows a diagram of the GSE with the UUT.

4. GSE Setup

Make sure all power switches on the MKVII WC GSE are turned off before connecting power to the system. Refer to the GSE Hardware User's Guide, Document 951-6517-603, for instructions on assembly of the system. Set up the MKVII WC GSE, test equipment, and UUT (refer to Figure 102).

5. GSE Power Requirements

Power requirements for the GSE are:

115 ±5 VAC, 60 -13HZ, +3Hz
115 ±3 VAC, 400 ±5Hz

6. Test Conditions

Unless otherwise specified, all tests shall be performed under factory or laboratory atmospheric conditions as specified in the following conditions:

Temperature:	Room Ambient 25 ±5°C
Altitude:	Normal ground.
Humidity:	Room ambient to 90% relative humidity.

1. MKVII WC GSE (P/N 951-6517-003, -004, or -005). This piece of test equipment is designed and manufactured by Sundstrand. For complete information on the tester, refer to the GSE Operation and Maintenance Manual (Document No. 012-0630-001).
2. MKVII WC ATP Software, Version 3.03 or higher (diskette) (P/N 998-1368-50X).
3. Fluke 8505A Digital Multimeter (DMM) with IEEE-488 and True RMS options.
4. Fluke Y8021 IEEE-488 GPIB Cable.
5. VGA color monitor for personal computer.
6. AST Premium/286 Personal Computer with 80286 Microprocessor.
7. GPIB Interface Card (P/N 300-1040-001).
8. Printer for personal computer.
9. RS232 Interface Card (P/N 300-1041-001).
10. Windows 3.1 Software (P/N 331-0006-004).
11. ATEasy Software (P/N 331-0017-001).
12. Microsoft Bus Mouse (P/N 300-0858-001).
13. MS-DOS Version 5.0 Software (P/N 331-0004-003).
14. Digital storage oscilloscope, Model 5440.
15. GSE Diagnostics software (P/N 998-1369-50X) for troubleshooting (optional).

MKVII Test Equipment
Figure 101

7. **Quality Assurance Provisions**

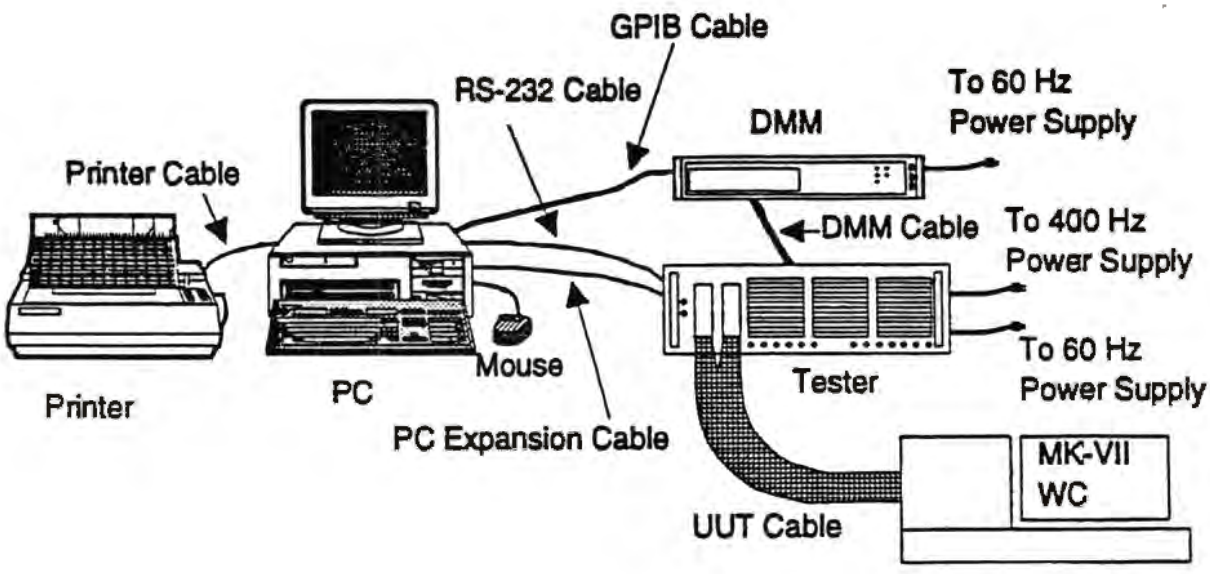
Inspect the UUT for damage before testing. Avoid contamination by smoke, dust, or other foreign substances.

8. **GSE Malfunction/Failure**

The ATP software performs a GSE self-test before testing. Any failures are logged to the current ATP test log and testing is aborted. The failed test equipment must be repaired or replaced.

9. **ATP Software Test Preparation**

The MKVII WC GSE ATP and Diagnostics software perform tests and housekeeping functions before ATP testing. These tests verify that the MKVII is capable of being tested and consist of an RS232 link test and a MKVII configuration test. Before starting an ATP, the MKVII hardware configuration



MKVII WC Test Equipment Setup
Figure 102

is read, flight time is read, the fault status is read, the flight history is read and cleared, and the nonvolatile memory (NVM) is cleared.

A. **RS232 Communication Link Test (ATP and Diagnostics)**

Because the ATP software uses an RS232 communications link with the MKVII during ATP testing, the ATP verifies that the MKVII can communicate over the RS232 link. During this test, the ATP software initializes the internal MKVII Terminal mode monitor and verifies that the MKVII responds. If the MKVII fails to respond, the failure is logged to the current ATP log file and the ATP is aborted.

B. **Configuration Test (ATP and Diagnostics)**

The GSE has its own unique program pin configuration which the MKVII recognizes as ATP mode. The ATP software interrogates the MKVII to verify that the WC detects that it is connected to the ATP tester. If the MKVII has a program pin failure, the failure is logged to the current ATP log and the ATP is aborted.

C. **Hardware Configuration Check (ATP and Diagnostics)**

Before an ATP is performed, and after the user has entered the MKVII part number, the ATP software reads the version numbers of the MKVII software (program module, data module, and analog/digital data acquisition board (ADDA) software). These versions are compared to the part number information to make sure they are the same. If the hardware does not match the given part number, the user is notified and the ATP is aborted.

D. **Flight Time Report (ATP and Diagnostics)**

MKVII units used by the military internally log accrued flight hours. On these military units, the ATP software reads this flight time and logs it to the current ATP log file. Flight hours are not logged by commercial units.

E. **Fault Status Report (ATP and Diagnostics)**

The MKVII maintains counters for various internal faults and failures which can occur during normal operation and that the MKVII detects during background self-testing. The ATP software reads these counters before testing and logs them to the current ATP file. These failures are logged to provide a permanent record of failures so that they will not be lost when the NVM is cleared. The optional Diagnostics software does not clear these counters when running a test.

Possible failures which could be reported are:

```
CPU test fail
RAM test fail
CRC ROM test fail
Waitstate test fail
Illegal interrupt
Operating system fail
Case branching error
Analog/digital converter fail
Dual ported RAM T/W test fail
Dual ported RAM throughput test fail
Watchdog timer test fail
Power up reset fail
Bad test value from PVM
System check fail
Bad command received
Biax #2 test fail
Biax #1 test fail
Serial bus #0 inactive
Serial bus #1 inactive
Serial bus #2 inactive
Serial bus #3 inactive
Received 429 label not valid or parity error
429 wraparound test fail
429 overrun error
```

F. **Flight History Check (ATP and Diagnostics)**

The flight history contains fault and warning occurrences from as many as 64 prior flights. Faults recognized by the flight history are those detected by the MKVII while the aircraft was airborne. Each fault message is followed by a list of flight numbers on which the fault occurred (for example, GLIDESLOPE WIRING FAULT, FLIGHT 1, 2, 45, 64). The flight history is stored in the processor/ voice/memory (PVM) NVM and is retrieved during an ATP. When an ATP is performed, the GSE logs the flight history information to the current ATP test log to provide a permanent record of the flight history, so that it will not be lost when the ATP clears the flight history. (Refer to paragraph G. for information about reading flight history without clearing the flight history.) The flight history messages are as follows:

```
Radio altitude
Baro rate
Glideslope
Accelerometer 1 and 2 (normal accelerometer)
Longitudinal Accelerometer 1 and 2
Airspeed 1 and 2
Pitch 1 and 2
```

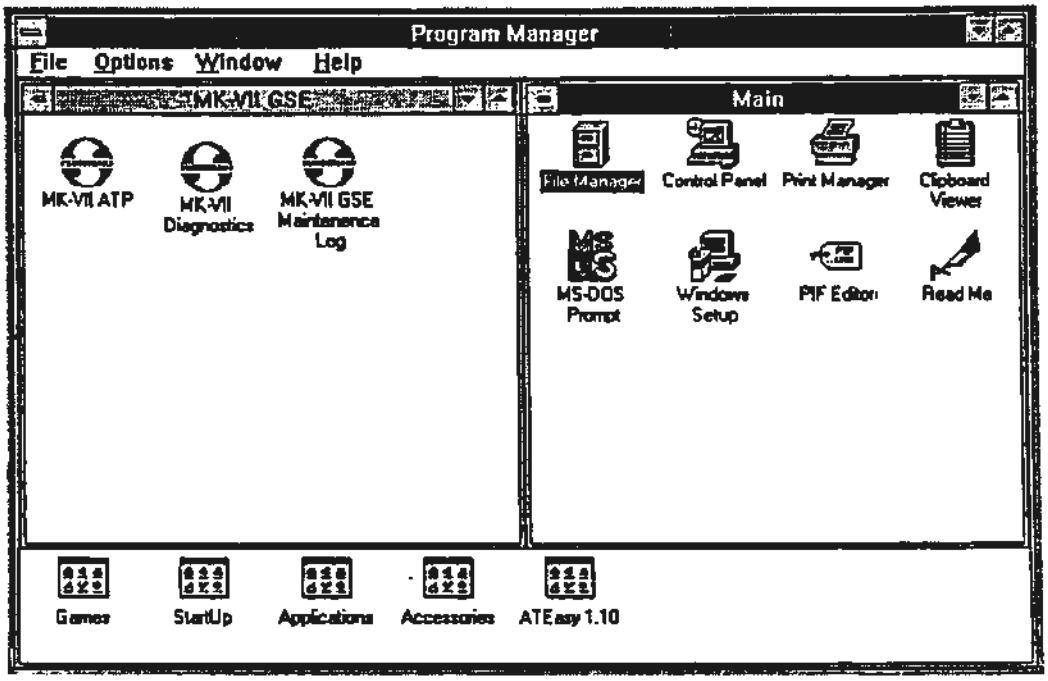
```
Pitch rate 1 and 2
Roll 1 and 2
Roll rate 1 and 2
Left flap angle
Right flap angle
Left angle of attack
Right angle of attack
Baro altitude (fine) 1 and 2
Course baro altitude 1 and 2
Air temperature 1 and 2
Localizer
Magnetic track angle
Runway course
Course (heading error)
Latitude
Longitude
Height rate (vertical speed) 1 and 2
Ahead flaps (slats) 1 and 2
Decision height
Glideslope invalid fault (low level validity)
Radio altitude invalid fault (low level validity)
Stall margin 1 and 2
Warning computer
Program pins wiring
Gear switch
Flap switch
Inop switch (GPWC test switch)
Guidance cancel switch 1
Guidance cancel switch 2
Guidance switch 1
Guidance switch 2
Glideslope cancel switch
Bus one inactive
Bus two inactive
Bus three inactive
Bus four inactive
```

G. **Flight History Clearing (ATP Only)**

Before starting an ATP, the ATP software clears the existing flight history. In order to read the flight history without clearing it, the optional Diagnostics software must be used. Upon entering the diagnostics software, press the F2 key or click on the START button. The diagnostics software reads the UUT flight history and logs it to the current test log but does not clear the flight history.

H. **NVM Clearing (ATP Only)**

The PVM NVM holds MKVII fault information as well as the flight history. Before starting an ATP, the PVM NVM is cleared. A test request #1 is sent to the MKVII. The ATP software verifies that the MKVII acknowledges the request and then cycles power to reset the MKVII RAM copies of the fault data. If the MKVII fails to acknowledge the test request, the failure is logged to the current ATP test log and the test is aborted. The optional Diagnostics software does not clear the NVM when running a test.



Windows Program Manager
Figure 103

10. **Acceptance Test Procedure (ATP)**

A. Perform the ATP according to the following steps:

(1) Connect the UUT cable to the UUT. Check all cable connections for the GSE. Turn on the MKVII WC GSE system power in the following order:

```
Turn on the 115 VAC 60Hz for the GSE.
Turn on the 115 VAC 60Hz for the PC.
Turn on the 115 VAC 400Hz for the GSE.
```

(2) Start Windows 3.1 by typing WIN at the C:>prompt.

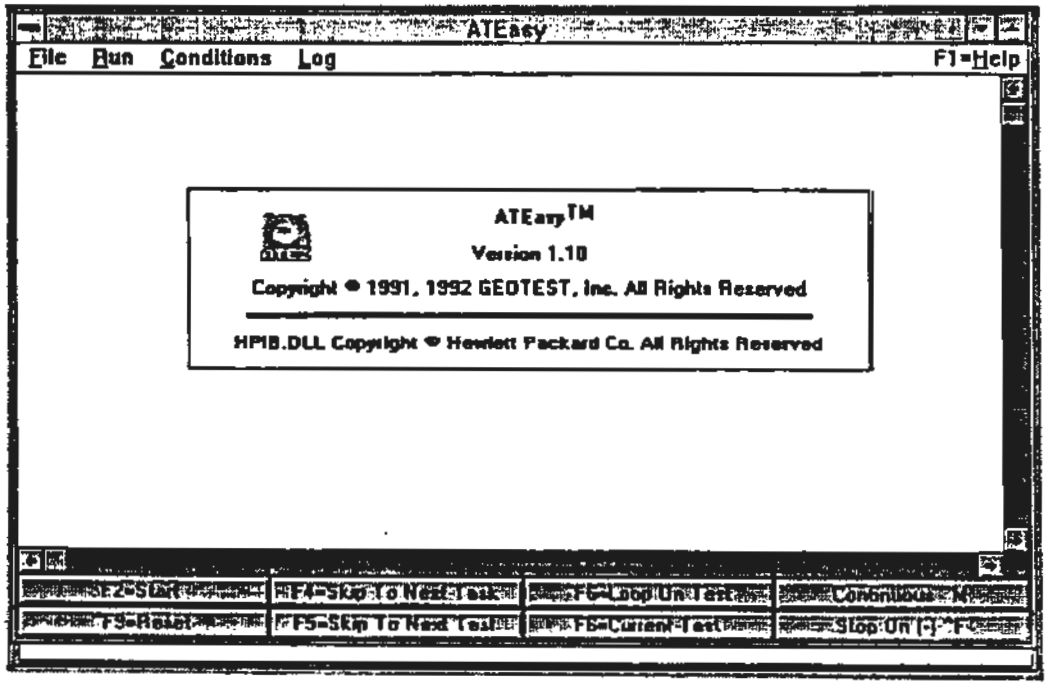
(3) After a brief delay, the Windows Program Manager screen (refer to Figure 103) should appear.

(4) Locate the MKVII ATP icon in the MKVII GSE group. Use the mouse to double-click the MKVII ATP icon to start the ATP software. An ATEasy sign-on (copyright) screen will appear (refer to Figure 104), followed by the password dialog screen (refer to Figure 105).

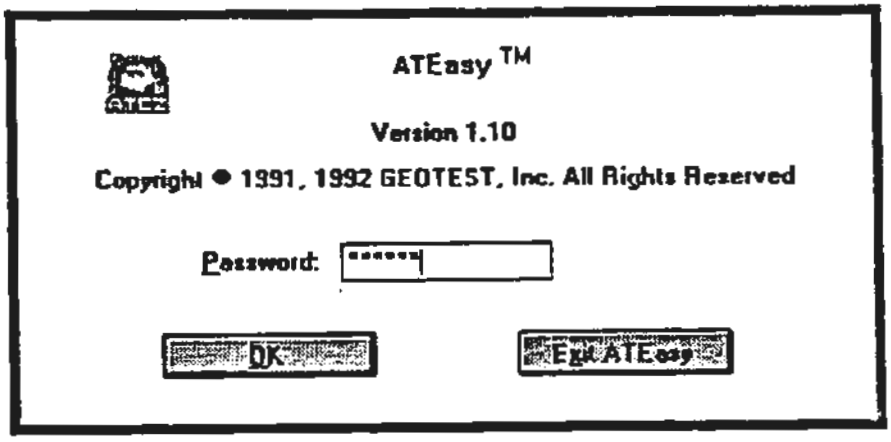
(5) Enter the user password. After the user password has been entered, the MKVII ATP test log initial information window (refer to Figure 106) will appear.

(6) In the MKVII ATP window, select the START button (or select F2). The ATEasy control window will compile messages and a PAUSE and ABORT button will appear (refer to Figure 107).

(7) After messages scroll by on the test log, the GSE master configuration window will appear



ATEasy Copyright Screen
Figure 104

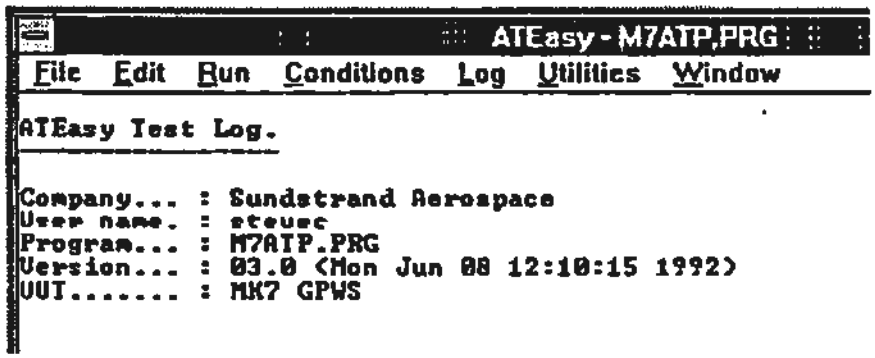


ATEasy Password Dialog
Figure 105

(refer to Figure 108).

(a) Make sure the GSE SOFTWARE VERSION NUMBER at the bottom of the master configuration window is 3.03 or higher.

(b) Make sure the MKVII MATRIX VERSION NUMBER at the bottom of the master configuration window is 01.02 or higher.


ATEasy - M7ATP.PRG
File Edit Run Conditions Log Utilities Window
ATEasy Test Log.
Company... : Sundstrand Aerospace
User name. : steuec
Program... : M7ATP.PRG
Version... : 03.0 (Mon Jun 08 12:10:15 1992)
UUT..... : MK7 GPWS

Test Log Initial Information
Figure 106

ATEasy Control Window
Figure 107

(c) Make sure that the MODE at the bottom of the master configuration window is ATP.

NOTE: *Refer to the MKVII GSE Software User's Manual, Document 998-1394-600, for more information on the master configuration window options.*

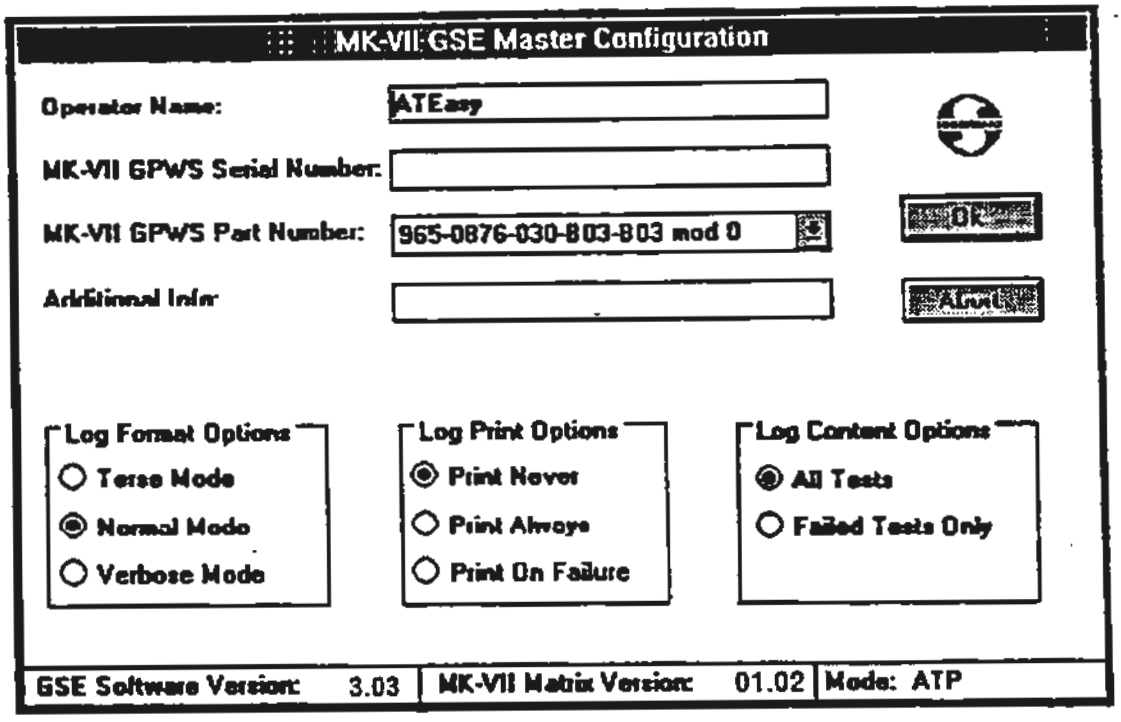
(8) In the master configuration window, enter the operator name (if different than what is displayed) and the UUT serial number (required).

(9) Use the TAB and ARROW keys (or the mouse) to select from the list of valid MKVII part numbers (refer to Figure 109).

(10) Use the ADDITIONAL INFO box on the master configuration window to type a line of optional information.

(11) Select the TERSE log format option, the PRINT NEVER log print option, and the log ALL TESTS option (refer to Figure 108).

NOTE: *To log higher levels of detail in the test log, set the LOG FORMAT OPTION to NORMAL or*



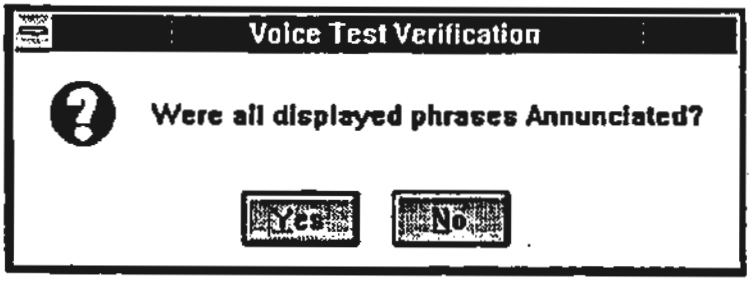
GSE Master Configuration
Figure 108

Part Number Scroll Box
Figure 109

VERBOSE MODE. To have the test log always print, select the PRINT ALWAYS log print option. The PRINT ON FAILURE log print option may also be selected. Any of these combinations are acceptable.

(12) Select OK by using the TAB key to highlight the OK button and selecting ENTER (or use the mouse to click the OK button). The MKVII WC GSE will automatically begin to test the UUT. The test takes approximately 35 minutes.

Voice Test Initial Dialog
Figure 110



Voice Test Conclusion Dialog
Figure 111

NOTE: *Test time can be shortened by selecting LOG FAILED TESTS ONLY or by making the size of the log window smaller (allowing only approximately five lines of data to be displayed).*

(13) After a short time, a dialog box will ask if the operator is ready for the voice test verification (refer to Figure 110). Select OK and listen to the audio tests.

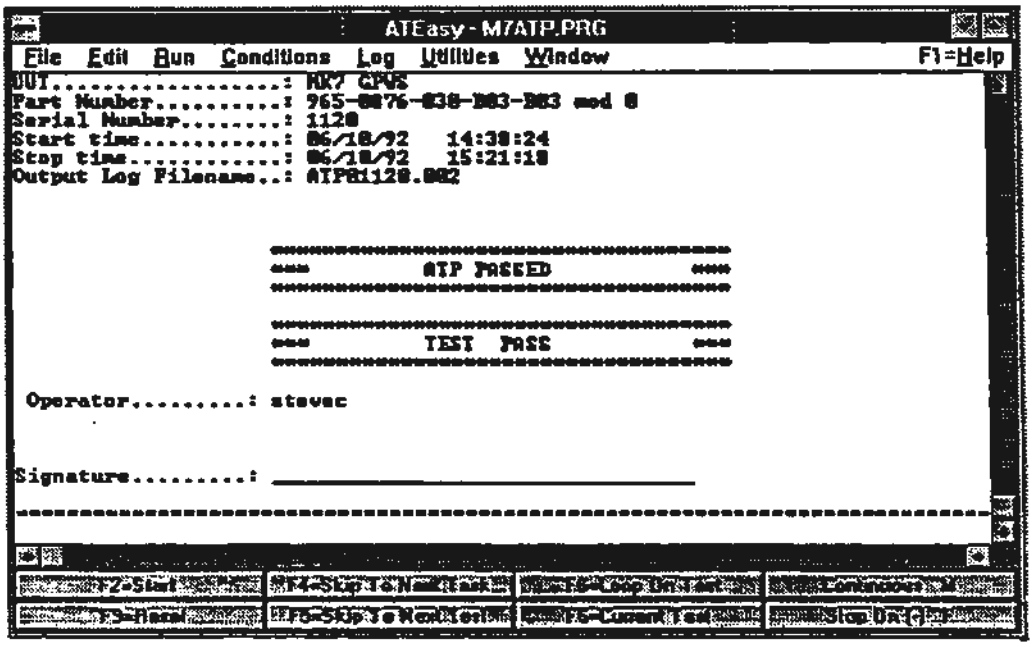
(14) After the voice test verification, a dialog box is displayed and asks if all the displayed voices were annunciated (refer to Figure 111). Select YES if they were.

NOTE: *The MKVII WC GSE will automatically continue testing the UUT without further operator interaction.*

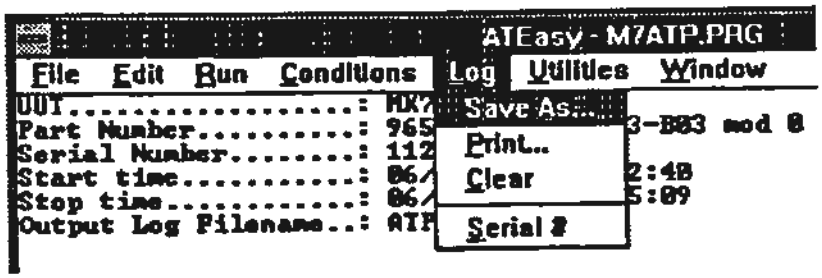
B. Review the Test Results

(1) At the end of the test cycle, the test log will indicate whether the ATP passed or failed (refer to Figure 112).

(2) If the ATP passed, select LOG from the menu, then select PRINT... to print out the test log



ATP Conclusion Test Log Screen
Figure 112



Test Log Print or Save Menu
Figure 113

(refer to Figure 113).

(3) If the ATP failed, the ATP software will list all failed tests at the end of the log. The user can also use the scroll bar at the right side of the test window to scroll through the tests and review the results. Save the test log to view at a later time, by selecting LOG from the menu and selecting SAVE AS... from the log menu (refer to Figure 113).

NOTE: In most cases, the repair technician can use the name of the failed test(s) to locate the

problem circuit in the schematic diagrams because many of the circuits are named similarly to the ATP names.

C. Printing a Paper Copy of the Test Results

A printed copy of the test results can be generated using the printer in the GSE system. Refer to the printer operation manual for instructions on using the GSE printer.

NOTE: *Do not attempt to run the ATP software while printing. This will cause RS232 failures to occur because of Windows latency.*

D. UUT Removal

(1) The ATP software automatically removes 400Hz power from the MKVII when testing is complete. Make sure that the GSE front panel 400Hz lamp is off.

(2) Unplug and remove the UUT.

(3) Exit ATEasy by double-clicking the ATEasy CLOSE bar in the upper left corner of the screen.

(4) Exit Windows by double-clicking the Windows CLOSE bar in the upper left corner of the screen.

(5) When the PC has returned to the C: prompt, turn off the PC 60Hz power, the GSE 60Hz power, and the GSE 400Hz power.

11. **Using the GSE System to Troubleshoot the MKVII**

The ATP software is designed to only perform the MKVII ATP. To troubleshoot the MKVII using the GSE system, it is necessary to have the optional MKVII GSE Diagnostics software (P/N 998-1369-50X).

NOTE: *All of the information in paragraphs 11. through 15. refer to Diagnostics software.*

A. ATP Tests

The ATP is made up of 48 tasks, with each consisting of a number of tests. When an ATP is performed, the ATP software automatically runs each task and all of the tests which belong to that task. During Diagnostics, all of the ATP tests are available to be run. The technician is able to pick and choose among the task and test list to compile a program profile for troubleshooting (refer to paragraph 11.B.). In addition to the program profiles, each test (where applicable) has the ability to accept custom test control from the user. Using the custom controls, the user can alter the input stimulus voltage and insert breakpoints to suspend testing to allow troubleshooting with the stimulus applied. Refer to the MKVII GSE Software User's Manual, Document 998-1394-600, for information on how to use the custom controls. Refer to Figure 114 for a list of ATP tasks and tests.

B. Program Profiles

To troubleshoot the MKVII using the GSE tester, the Diagnostics software allows the user to define program profiles by selecting EDIT from the main menu and selecting the program profiles choice (refer to Figure 115). These program profiles are selected groups of tasks and tests which will be executed when software is started by either pressing the F2 key or clicking on the START button on the main ATEasy screen. Refer to the MKVII GSE Software User's Manual, Document 998-1394-600, and the ATEasy User's Manual for information on creating and using program profiles.

C. ATP and Diagnostics Test Reports

Refer to the MKVII GSE Software User's Manual, Document 998-1394-600, for information

about the test log files which are generated during ATP and Diagnostics tests.

D. GSE Maintenance Log

The ATP and Diagnostics software records all GSE system errors to a maintenance log file. Refer to the MKVII GSE Software User's Manual, Document 998-1394-600, for information on the system maintenance log file.

12. **Troubleshooting the MKVII**

The following information assumes the UUT has failed the ATP and the technician must identify the failed components. The technician may use standard troubleshooting practices and equipment to locate the failed components.

Diagnostic testing (using the RS232 Terminal interface) and examples of failures and the troubleshooting sequence are included in paragraphs 13. and 14. Examples are included to give an overview of troubleshooting methods. Because the MKVII is versatile and complex, complete troubleshooting instructions for every possible circumstance are not included in this manual.

NOTE: *Do not use any form of circuit cooler to troubleshoot the boards. Circuit cooler removes the conformal coating.*

NOTE: *Conformal coating on the ADDA, PVM, and power supply board is applied with a heavy coat. Make sure to pierce through the conformal coating when using a digital multimeter (DMM) or oscilloscope to take a measurement.*

Schematics, data book pin outs, memory maps and addresses, and PAL equations are listed at the end of TESTING AND TROUBLESHOOTING to assist the technician using the GSE to test operation of specific circuits.

13. **Using the MKVII RS232 Terminal Interface**

The following paragraphs A. through L. define the configuration, initialization, and use of the MKVII WC GSE RS232 Terminal interface. A complete listing of commands and operation instructions can be obtained after initialization by entering a question mark (?) at the prompt. All data supplied by the user must be in capital letters. All addresses and data values must be in hexadecimal. (Hexadecimal numbers are identified by either a leading 0x or an ending H: hexadecimal (HEX) 55 = 0x55 = 55H.)

A. **Powering the UUT**

(1) Start the MKVII WC GSE Diagnostics program (through Windows or ATEasy).

(2) From the main menu, select DIAGNOSTICS.

(3) After the Diagnostics menu appears, select MK7 CONTROLS.

(4) When the MKVII control panel appears, select MKVII POWER, POWER ON.

NOTE: *Remove power by performing steps (1) through (4) listed above, except select MKVII POWER, POWER OFF from the MKVII control panel.*

TASK #	TEST
TASK 1	**Initialization**
	TEST 1 Low line
	TEST 2 Warm start
	TEST 3 Cold start
TASK 2	**Audio**
	TEST 1 Voice Annunciation
	TEST 2 600 Ohm Audio Output #1 Test #1
	TEST 3 600 Ohm Audio Output #1 Test #2
	TEST 4 600 Ohm Audio Output #1 Test #3
	TEST 5 600 Ohm Audio Output #2 Test #1
	TEST 6 600 Ohm Audio Output #2 Test #2
	TEST 7 600 Ohm Audio Output #2 Test #3
	TEST 8 8 Ohm Audio Output Test #1
	TEST 9 8 Ohm Audio Output Test #2
	TEST 10 8 Ohm Audio Output Test #3
TASK 3	**Power Supply**
	TEST 1 +24 VDC Test #1 (115 VAC)
	TEST 2 +24 VDC Ripple Test #1 (115 VAC)
	TEST 3 -24 VDC Test #1 (115 VAC)
	TEST 4 -24 VDC Ripple Test #1 (115 VAC)
	TEST 5 +24 VDC Test #2 (104 VAC)
	TEST 6 +24 VDC Ripple Test #2 (104 VAC)
	TEST 7 -24 VDC Test #2 (104 VAC)
	TEST 8 -24 VDC Ripple Test #2 (104 VAC)
	TEST 9 +5 VDC A/D Reference Test
	TEST 10 +5 VDC A/D Reference Ripple Test
TASK 4	**Ground Pins**
	TEST 1 Captain's Guidance Common
	TEST 2 First Officer's Guidance Common
	TEST 3 +5VDC Ground
TASK 5	**Lamp ON/OFF**
	TEST 1 Unpowered Lamp Test
	TEST 2 Lamp #1 ON Test
	TEST 3 Lamp #2 ON Test
	TEST 4 Lamp #3 ON Test
	TEST 5 Lamp #4 ON Test
	TEST 6 Lamp #5 and #6 ON Test
	TEST 7 Lamp #7 ON Test (Type 1,3)
	TEST 8 Lamp #7 ON Test #1 (Type 2)
	TEST 9 Lamp #7 ON Test #2 (Type 2)
	TEST 10 Lamp #7 ON Test #3 (Type 2)
	TEST 11 Lamp #8 ON Test
	TEST 12 Lamp #9 ON Test
	TEST 13 Lamp #10 ON Test

Tasks and Tests
Figure 114 (Sheet 1)

TASK #	TEST
	TEST 14 Lamp #11 ON Test
	TEST 15 Lamp #12 ON Test
	TEST 16 Lamp #13 ON Test
TASK 6	**Discrete Outputs**
	TEST 1 Discrete Output #1 OFF Test #1
	TEST 2 Discrete Output #1 OFF Test #2
	TEST 3 Discrete Output #1 ON Test
	TEST 4 Discrete Output #2 OFF Test #1
	TEST 5 Discrete Output #2 OFF Test #2
	TEST 6 Discrete Output #2 ON Test
	TEST 7 Discrete Output #3 ON Test
	TEST 8 Discrete Output #4 ON Test
	TEST 9 Discrete Output #5 ON Test
	TEST 10 Discrete Output #6 ON Test
TASK 7	**PVM Analog Outputs**
	TEST 1 Analog Output #1 and #4 On Test
	TEST 2 Analog Output #1 and #4 Off Test
	TEST 3 Analog Output #2 and #5 On Test
	TEST 4 Analog Output #2 and #5 Off Test
	TEST 5 Analog Output #3 and #6 On Test
	TEST 6 Analog Output #3 and #6 Off Test
TASK 8	**PVM Analog Inputs**
	TEST 1 Analog Input #1 Test #1
	TEST 2 Analog Input #1 Test #2
	TEST 3 Analog Input #2 Test #1
	TEST 4 Analog Input #2 Test #2
TASK 9	**Built In Test**
	TEST 1 PVM Incremental CPU Test
	TEST 2 PVM Incremental RAM Test
	TEST 3 PVM Incremental ROM CRC Test
	TEST 4 PVM Watchdog Timer Test
	TEST 5 PVM Wait State Hardware Test
	TEST 6 PVM Analog Hardware Test
	TEST 7 PVM Warmstart Circuit Test
	TEST 8 PVM Voice Test
	TEST 9 PVM Data Module CRC Test
	TEST 10 PVM Verify NVM Test
	TEST 11 PVM Operating System Test
	TEST 12 Dual Port RAM Test
	TEST 13 ADDA Wait State Test
	TEST 14 ADDA A/D Converter Test
	TEST 15 ADDA Watchdog Timer Test
	TEST 16 ADDA Local RAM Test
	TEST 17 ADDA ROM CRC Test

Tasks and Tests
Figure 114 (Sheet 2)

TASK #	TEST
	TEST 18 ADDA CPU Test
TASK 10	**ADDA Outputs (J2-K10)**
	TEST 1 Analog Output Test #1
	TEST 2 Analog Output Test #2
	TEST 3 Analog Output Test #3
TASK 11	**ARINC 429**
	TEST 1 ARINC 429 BIT Test
	TEST 2 ARINC 429 Output Test #1
	TEST 3 ARINC 429 Output Test #2
	TEST 4 ARINC 429 Input Test #1 Ch #0
	TEST 5 ARINC 429 Input Test #1 Ch #1
	TEST 6 ARINC 429 Input Test #1 Ch #2
	TEST 7 ARINC 429 Input Test #1 Ch #3
	TEST 8 ARINC 429 Input Test #2 Ch #0
	TEST 9 ARINC 429 Input Test #2 Ch #1
	TEST 10 ARINC 429 Input Test #2 Ch #2
	TEST 11 ARINC 429 Input Test #2 Ch #3
TASK 12	**2-Wire #1** (J1B-20 (+), J1B-21 (-): OC Rad Alt)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Positive Open Wire Test
	TEST 5 Negative Open Wire Test
TASK 13	**2-Wire #2** (J1B-19 (+), J2-B3 (-): Rad Alt Val)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
TASK 14	**2-Wire #3** (J1A-22 (+), J1A-23 (-): OC GS Dev)
	TEST 1 High Level: Positive Gain Test
	TEST 2 High Level: Negative Gain Test
	TEST 3 High Level: Positive Filter Test
	TEST 4 High Level: Negative Filter Test
	TEST 5 Low Level: Positive Gain Test
	TEST 6 Low Level: Negative Gain Test
	TEST 7 Low Level: Positive Filter Test
	TEST 8 Low Level: Negative Filter Test
	TEST 9 Low Level: Positive Open Wire Test
	TEST 10 Low Level: Negative Open Wire Test

Tasks and Tests
Figure 114 (Sheet 3)

TASK #	TEST
TASK 15	**2-Wire #4** (J1A-19 (+), J1A-20 (–): GS Val)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 16	**2-Wire #5** (J1B-28 (+), J1B-30 (–), J18-29 (GND): Baro Alt Rate #1)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
	TEST 5 Positive Open Wire Test
	TEST 6 Negative Open Wire Test
TASK 17	**2-Wire #6** (J2-K4 (+), J2-K7 (–), J2-K5 (GND): Baro Alt Rate #2)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 18	**2-Wire #7** (J1A-39 (+), J1A-40 (–): DC Mach)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
	TEST 4 Positive Filter Test
	TEST 5 Negative Filter Test
TASK 19	**2-Wire #8** (J2-J4 (+), J2-J5 (–): DC Sat)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
	TEST 4 Positive Filter Test
	TEST 5 Negative Filter Test
TASK 20	**2-Wire #9** (J2-J7 (+), J2-J6 (–): DC Sat Ref)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 21	**2-Wire #10** (J2-H1 (+), J2-H2 (–): DC AOA #1)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
	TEST 4 Positive Filter Test
	TEST 5 Negative Filter Test

TASK #	TEST
TASK 22	**2-Wire #11** (J2-C1 (+), J2-C2 (–): DC AOA #2)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
	TEST 4 Positive Filter Test
	TEST 5 Negative Filter Test
TASK 23	**2-Wire #12** (J2-H12 (+), J2-H13 (–): DC Norm Acc #1)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 24	**2-Wire #13** (J2-E4 (+), J2-E5 (–): DC Norm Acc #2)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 25	**2-Wire #14** (J2-H14 (+), J2-H15 (–): DC Long Acc #1)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 26	**2-Wire #15** (J2-E6 (+), J2-E7 (–): DC Long Acc #2)
	TEST 1 Positive Gain Test
	TEST 2 Negative Gain Test
	TEST 3 Positive Filter Test
	TEST 4 Negative Filter Test
TASK 27	**2-Wire #16** (J2-H4 (+), J2-H5 (–): DC Spare #1)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
	TEST 4 Positive Filter Test
	TEST 5 Negative Filter Test
TASK 28	**2-Wire #17** (J2-D6 (+), J2-D7 (–): DC Spare #2)
	TEST 1 Positive Gain Test (no offset)
	TEST 2 Positive Gain Test (5V offset)
	TEST 3 Negative Gain Test
	TEST 4 Positive Filter Test
	TEST 5 Negative Filter Test

TASK #	TEST
TASK 29	**2-Wire #18** (J2-J1 (+), J2-J2 (–): DC Stall Margin #1) TEST 1 Positive Gain Test (no offset) TEST 2 Positive Gain Test (5V offset) TEST 3 Negative Gain Test TEST 4 Positive Filter Test TEST 5 Negative Filter Test
TASK 30	**2-Wire #19** (J2-C13 (+), J2-C14 (–): DC Stall Margin #2) TEST 1 Positive Gain Test (no offset) TEST 2 Positive Gain Test (5V offset) TEST 3 Negative Gain Test TEST 4 Positive Filter Test TEST 5 Negative Filter Test
TASK 31	**2-Wire #20** (J2-J13 (+), J2-J14 (–): Flap Pos #1) TEST 1 Positive Gain Test TEST 2 Negative Gain Test TEST 3 Positive Filter Test TEST 4 Negative Filter Test
TASK 32	**2-Wire #21** (J2-D1 (+), J2-D2 (–): Flap Pos #2) TEST 1 Positive Gain Test TEST 2 Negative Gain Test TEST 3 Positive Filter Test TEST 4 Negative Filter Test
TASK 33	**2-Wire #22** (J2-K6 (+), J2-K7 (–): Baro Rate Ref #2) TEST 1 Positive Gain Test TEST 2 Negative Gain Test
TASK 34	**2-Wire #23** (J2-K4 (+), J2-K5 (–): AC Baro Alt Rate #2) TEST 1 Positive Gain Test TEST 2 Negative Gain Test TEST 3 Positive Open Wire (Type 1) TEST 4 Positive Open Wire (Type 2,3) TEST 5 Negative Open Wire (Type 1) TEST 6 Negative Open Wire (Type 2,3)
TASK 35	**2-Wire #24** (J1B-37 (+), J1B-38 (–): AC Baro Alt Rate #1) TEST 1 Positive Gain Test TEST 2 Negative Gain Test TEST 3 Positive Open Wire (Type 1) TEST 4 Positive Open Wire (Type 2,3) TEST 5 Negative Open Wire (Type 1) TEST 6 Negative Open Wire (Type 2,3)

Tasks and Tests
Figure 114 (Sheet 6)

TASK #	TEST	
TASK 36	**2-Wire #25** (J1B-39 (+), J1B-40 (–): AC Baro Rate Ref #1)	
	TEST 1 Positive Gain Test	
	TEST 2 Negative Gain Test	
TASK 37	**2-Wire #26** (J2-H6 (+), J2-H7 (–): AC Baro Alt)	
	TEST 1 Positive Gain Test	
	TEST 2 Negative Gain Test	
TASK 38	**2-Wire #27** (J2-J4 (+), J2-J5 (–): DC SAT Gain)	
	TEST 1 Positive Gain Test	
	TEST 2 Negative Gain Test	
TASK 39	**2-Wire #28** (J2-J6 (+), J2-J7 (–): AC SAT Ref)	
	TEST 1 Positive Gain Test	
	TEST 2 Negative Gain Test	
TASK 40	**Gain Select**	
	TEST 1 DC Gain Select Test #1	
	TEST 2 DC Gain Select Test #2	
TASK 41	**2-Wire Reference**	
	TEST 1 Reference Test #1, Test #1	J1B-39, J1B-40: Baro Rate Ref #1
	TEST 2 Reference Test #1, Test #2	
	TEST 3 Reference Test #1, Test #3	
	TEST 4 Reference Test #1, Test #4	
	TEST 5 Reference Test #2, Test #1	J2-K6, J2-K7: Baro Rate Ref #2
	TEST 6 Reference Test #2, Test #2	
	TEST 7 Reference Test #2, Test #3	
	TEST 8 Reference Test #2, Test #4	
	TEST 9 Reference Test #3, Test #1	J2-J6, J2-J7: SAT Ref
	TEST 10 Reference Test #3, Test #2	
	TEST 11 Reference Test #3, Test #3	
	TEST 12 Reference Test #3, Test #4	
	TEST 13 Reference Test #4, Test #1	J2-H10, J2-H11: Spare Ref #1
	TEST 14 Reference Test #4, Test #2	
	TEST 15 Reference Test #4, Test #3	
	TEST 16 Reference Test #4, Test #4	
	TEST 17 Reference Test #5, Test #1	J2-E8, J2-E9: Spare Ref #2
	TEST 18 Reference Test #5, Test #2	
	TEST 19 Reference Test #5, Test #3	
	TEST 20 Reference Test #5, Test #4	

TASK #	TEST	
TASK 42	**3-Wire Attenuation**	
	TEST 1 3-Wire #1 Test #1	J1A-36, J1A-37, J1A-38: Mach/CAS
	TEST 2 3-Wire #1 Test #2	
	TEST 3 3-Wire #1 Test #3	
	TEST 4 3-Wire #2 Test #1	J2-J13, J2-J14, J2-J15: Flaps #1
	TEST 5 3-Wire #2 Test #2	
	TEST 6 3-Wire #2 Test #3	
	TEST 7 3-Wire #3 Test #1	J2-K1, J2-K2, J2-K3: Pitch #1
	TEST 8 3-Wire #3 Test #2	
	TEST 9 3-Wire #3 Test #3	
	TEST 10 3-Wire #4 Test #1	J2-K13, J2-K14, J2-K15: Roll #1
	TEST 11 3-Wire #4 Test #2	
	TEST 12 3-Wire #4 Test #3	
	TEST 13 3-Wire #5 Test #1	J2-H1, J2-H2, J2-H3: AOA #1
	TEST 14 3-Wire #5 Test #2	
	TEST 15 3-Wire #5 Test #3	
	TEST 16 3-Wire #6 Test #1	J2-J1, J2-J2, J2-J3: Stall Margin #1
	TEST 17 3-Wire #6 Test #2	
	TEST 18 3-Wire #6 Test #3	
	TEST 19 3-Wire #7 Test #1	J2-J8, J2-J9, J2-J10: Spare #1
	TEST 20 3-Wire #7 Test #2	
	TEST 21 3-Wire #7 Test #3	
	TEST 22 3-Wire #8 Test #1	J1A-8, J1A-9, J1A-10: Baro Alt Fine
	TEST 23 3-Wire #8 Test #2	
	TEST 24 3-Wire #8 Test #3	
	TEST 25 3-Wire #9 Test #1	J2-D2, J2-D1, J2-D3: Flaps #2
	TEST 26 3-Wire #9 Test #2	
	TEST 27 3-Wire #9 Test #3	
	TEST 28 3-Wire #10 Test #1	J2-D14, J2-D13, J2-D15: Pitch #2
	TEST 29 3-Wire #10 Test #2	
	TEST 30 3-Wire #10 Test #3	
	TEST 31 3-Wire #11 Test #1	J2-E2, J2-E1, J2-E3: Roll #2
	TEST 32 3-Wire #11 Test #2	
	TEST 33 3-Wire #11 Test #3	
	TEST 34 3-Wire #12 Test #1	J2-C2, J2-C1, J2-C3: AOA #2
	TEST 35 3-Wire #12 Test #2	
	TEST 36 3-Wire #12 Test #3	
	TEST 37 3-Wire #13 Test #1	J2-C14, J2-C13, J2-C15: Stall Margin #2
	TEST 38 3-Wire #13 Test #2	
	TEST 39 3-Wire #13 Test #3	
	TEST 40 3-Wire #14 Test #1	J2-D9, J2-D8, J2-D10: Spare #2
	TEST 41 3-Wire #14 Test #2	
	TEST 42 3-Wire #14 Test #3	

TASK #	TEST		
TASK 43	**3-Wire Switch**		
	TEST 1	AC/DC #1 Test (X-Z)	
	TEST 2	AC/DC #1 Test (Y-Z)	
	TEST 3	AC/DC #2 Test (X-Z)	
	TEST 4	AC/DC #2 Test (Y-Z)	
TASK 44	**Synchro**		
	TEST 1	Synchro #1 Test #1	J1A-36, J1A-37, J1A-38: Mach/CAS
	TEST 2	Synchro #1 Test #2	
	TEST 3	Synchro #2 Test #1	J2-J13, J2-J14, J2-J15: Flaps #1
	TEST 4	Synchro #2 Test #2	
	TEST 5	Synchro #3 Test #1	J2-K1, J2-K2, J2-K3: Pitch #1
	TEST 6	Synchro #3 Test #2	
	TEST 7	Synchro #4 Test #1	J2-K13, J2-K14, J2-K15: Roll #1
	TEST 8	Synchro #4 Test #2	
	TEST 9	Synchro #5 Test #1	J2-H1, J2-H2, J2-H3: AOA #1
	TEST 10	Synchro #5 Test #2	
	TEST 11	Synchro #6 Test #1	J2-J1, J2-J2, J2-J3: Stall Margin #1
	TEST 12	Synchro #6 Test #2	
	TEST 13	Synchro #7 Test #1	J2-J8, J2-J9, J2-J10: Spare #1
	TEST 14	Synchro #7 Test #2	
	TEST 15	Synchro #8 Test #1	J1A-8, J1A-9, J1A-10: Baro Alt Fine
	TEST 16	Synchro #8 Test #2	
	TEST 17	Synchro #9 Test #1	J2-D2, J2-D1, J2-D3: Flaps #2
	TEST 18	Synchro #9 Test #2	
	TEST 19	Synchro #10 Test #1	J2-D14, J2-D13, J2-D15: Pitch #2
	TEST 20	Synchro #10 Test #2	
	TEST 21	Synchro #11 Test #1	J2-E2, J2-E1, J2-E3: Roll #2
	TEST 22	Synchro #11 Test #2	
	TEST 23	Synchro #12 Test #1	J2-C2, J2-C1, J2-C3: AOA #2
	TEST 24	Synchro #12 Test #2	
	TEST 25	Synchro #13 Test #1	J2-C14, J2-C13, J2-C15: Stall Margin #2
	TEST 26	Synchro #13 Test #2	
	TEST 27	Synchro #14 Test #1	J2-D9, J2-D8, J2-D10: Spare #2
	TEST 28	Synchro #14 Test #2	

TASK #	TEST

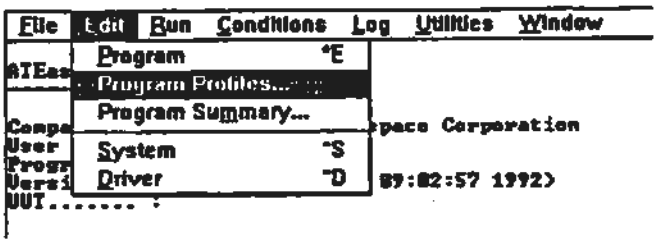
TASK 45 Program Pins

TEST 1 Program Pin Test #1
TEST 2 Program Pin Test #2
TEST 3 Program Pin Test #3
TEST 4 Program Pin Test #4
TEST 5 Program Pin Test #5
TEST 6 Program Pin Test #6
TEST 7 Program Pin Test #7
TEST 8 Program Pin Test #8
TEST 9 Program Pin Test #9
TEST 10 Program Pin Test #10
TEST 11 Program Pin Test #11
TEST 12 Program Pin Test #12
TEST 13 Program Pin Test #13
TEST 14 Program Pin Test #14
TEST 15 Program Pin Test #15
TEST 16 Program Pin Test #16
TEST 17 Program Pin Test #17
TEST 18 Program Pin Test #18
TEST 19 Program Pin Test #19
TEST 20 Program Pin Test #20
TEST 21 Program Pin Test #21
TEST 22 Program Pin Test #22
TEST 23 Program Pin Test #23
TEST 24 Program Pin Test #24
TEST 25 Program Pin Test #25
TEST 26 Program Pin Test #26
TEST 27 Program Pin Test #27
TEST 28 Program Pin Test #28

TASK 46 Ground Discretes

TEST 1 Ground Discrete Test #1
TEST 2 Ground Discrete Test #2
TEST 3 Ground Discrete Test #3
TEST 4 Ground Discrete Test #4
TEST 5 Ground Discrete Test #5
TEST 6 Ground Discrete Test #6
TEST 7 Ground Discrete Test #7
TEST 8 Ground Discrete Test #8
TEST 9 Ground Discrete Test #9
TEST 10 Ground Discrete Test #10
TEST 11 Ground Discrete Test #11
TEST 12 Ground Discrete Test #12
TEST 13 Ground Discrete Test #13
TEST 14 Ground Discrete Test #14
TEST 15 Ground Discrete Test #15

TASK #	TEST
TASK 47	**28V Discretes**
	TEST 1 28V Discrete Test #1
	TEST 2 28V Discrete Test #2
	TEST 3 28V Discrete Test #3
	TEST 4 28V Discrete Test #4
	TEST 5 28V Discrete Test #5
	TEST 6 28V Discrete Test #6
	TEST 7 28V Discrete Test #7
	TEST 8 28V Discrete Test #8
	TEST 9 28V Discrete Test #9
	TEST 10 28V Discrete Test #10
	TEST 11 28V Discrete Test #11
	TEST 12 28V Discrete Test #12
	TEST 13 28V Discrete Test #13
	TEST 14 28V Discrete Test #14
	TEST 15 28V Discrete Test #15
TASK 48	**Programmable Discretes**
	TEST 1 Programmable Discrete #1 Test #1
	TEST 2 Programmable Discrete #1 Test #2
	TEST 3 Programmable Discrete #2 Test #1
	TEST 4 Programmable Discrete #2 Test #2
	TEST 5 Programmable Discrete #3 Test #1
	TEST 6 Programmable Discrete #3 Test #2
	TEST 7 Programmable Discrete #4 Test #1
	TEST 8 Programmable Discrete #4 Test #2
	TEST 9 Programmable Discrete #5 Test #1
	TEST 10 Programmable Discrete #5 Test #2
	TEST 11 Programmable Discrete #6 Test #1
	TEST 12 Programmable Discrete #6 Test #2



Program Profiles Choice
Figure 115

B. Terminal Interface Specification

The MKVII supplies a high-speed, full duplex RS232 interface intended for test support. The interface configuration is as follows:

```
19.2K Baud
8 Data Bits
1 Stop Bit
No Parity
Xon/Xoff Software Flow Control
```

The interface requires a minimum pin 2, 3, and 7 cable connection (part of the GSE system). The MKVII WC GSE connects the GSE PC COM2 port to the RS232 communications port. Communication with the UUT is accomplished with the MKVII WC GSE system and the MKVII WC GSE Diagnostics software by performing the following steps:

NOTE: UUT power must be applied before attempting RS232 communications.

(1) From the MKVII WC GSE Diagnostics main menu, select DIAGNOSTICS.

(2) After the Diagnostics menu appears, select MK7 MONITOR. A MKVII configured version of Windows Terminal will appear. While in Terminal, all characters typed are sent to the PC COM port. The MKVII response (if any) will then be displayed on the screen.

C. Terminal Mode Initialization

The Terminal interface is initialized by transmitting the following character sequence to the UUT.

Character	Hex Value
CTRL-Z	1A
CR	0D

Enter this initialization sequence manually by holding the CTRL key down and pressing the Z key. After these keys are released, press the ENTER key. The initialization can also be invoked by selecting the INITIALIZE push button at the bottom of the Terminal screen.

When initialization is completed, a header and prompt (>) will be transmitted by the UUT and displayed on the screen. Initialization can be repeated at any time and should be performed when problems arise with the interface.

D. **PVM Command Interface**

Troubleshooting requires the use of change word (CW), display word (DW), output byte (OB), and input byte (IB) commands.

(1) The CW command is used to modify RAM variables on the PVM subsystem. The user is prompted to supply the hexadecimal address and desired value. In the following example, the word at address 0x8F00 is changed from 0x0000 to 0x1234. (Press the ENTER key to move to the next word if no change is wanted.) The function displays confirmation of the change and moves to the next memory location. The function is terminated by sending CTRL-U (0x15) (hold the CTRL key down and press the U key).

```
EXAMPLE:

>CW
Address? 8F00
8F00:  0000/1234
8F00:  1234
8F02:  1000/ U
```

(2) (2) The DW command is used to display a range of random access memory (RAM) on the PVM subsystem. The user is prompted to supply the hexadecimal address and the number of words (from 0x01 to 0xA0). If less than nine words are requested, the monitor will display the RAM values in 'update mode'. Any changes to the specified locations are displayed as they occur. Update mode is terminated by sending CTRL-O (0x10) (hold the CTRL key down and press the O key).

```
EXAMPLE:

>DW
Address? 8000
How many? 0F
8000:  1234 D000 1111 1222 1234 A55A 6ADF 21A0
8008:  5555 6666 4444 1111 1112 3333 AAAA
>
```

(3) The OB command is used to write byte values to PVM normal input/output (I/O) ports. The user is prompted to supply the I/O port address and the value to be written.

```
EXAMPLE:

>OB
Address? 5021
5021:  30
>
```

(4) The IB command is used to read byte values from PVM normal I/O ports. The user is prompted to supply the desired port address. This function displays the port value in 'update mode'. Any changes to the specified port are displayed as they occur. Update

mode is terminated by sending CTRL-O (0x10) (hold the CTRL key down and press the O key).

EXAMPLE:

```
>IB
Address? 5021
5021:  AD
```

E. **PVM Indirect Address Table**

The PVM software contains an indirect address table located in read only memory (ROM) at address 0010H (refer to Figure 116). Variables like PVMCOM can be relocated due to software changes. Its correct address must be determined through the table. The structure of the table is constant with additions appended to the end of the list. Each entry is a 16-bit word address pointer. When troubleshooting with the RS232 interface, use entries from this table. The table for the current software release can be retrieved using the following DW command:

```
>DW
Address? 0010
How many? 70
```

F. **Special PVM Debugging Mechanisms**

The PVM subsystem contains several variable locations that are useful for debugging purposes. The addresses of these variables are found in the PVM indirect address table.

G. **Digital-to-Analog Converter (DAC) Programming**

The guidance DAC on the PVM can be commanded to output values by setting the driver variables DAOUT1, DAOUT2, and DAOUT3 (refer to the PVM indirect address table) corresponding to pitch command, roll command, and fast/slow outputs. The outputs are scaled by the flight director gain factors found in three consecutive words beginning at the address of DACPAR (refer to the PVM indirect address table) corresponding to the pitch command gain, roll command gain, and fast/slow gain in that order.

H. **Analog-to-Digital Converter (ADC) Read Back**

The guidance read back ADC monitors the PVM continuously. The most recently gathered values are available as 14-byte wide values stored at address ADCDAT (refer to the PVM indirect address table). Figure 117 describes the order of the table.

I. **ADDA Interface**

The Terminal interface is a function supplied by the PVM subsystem and it contains facilities for performing similar functions on the ADDA board. This is done through a command port (PVMCOM) located in dual ported RAM (refer to the PVM indirect address table for the actual address). Through this command port, the ADDA is commanded to set and display the contents of ADDA RAM, ROM, and I/O ports.

J. **ADDA Command Port Definition**

The PVMCOM command port is comprised of eight 16-bit words, the first of which is the command word followed sequentially by parameters P1 through P7. To operate the command port, all required parameters are loaded into P1 through P7. The command word is then written with the desired command number. P1 through P7 are variable parameters. The number of parameters used and their function depend on the ADDA command to be used (refer to Figure 118).

REGISTER	OFFSET	DESCRIPTION
ADACFG	0 (0x0010)	DUAL PORT RAM ADDA DATA CONFIGURATION TABLE (300 WORDS)
ADAFLG	2	DUAL PORT RAM ADDA STATUS FLAGS WORD
ADAFLT	4	DUAL PORT RAM ADDA FAULT FLAGS WORDS (4 WORDS)
ADCDAT	6	PVM A-TO-D CONVERTER (ADC) INPUT DATA TABLE (14 BYTES)
ATP	8	ATP MODE BOOLEAN BYTE
CNFFLG	10	CONFIGURATION STATUS FLAGS BYTE
DACPAR	12	PVM DAC SCALE FACTOR DATA TABLE POINTER (3 WORDS)
DAOUT1	14	PVM ANALOG OUTPUT CHANNEL #1 AND #4 CONTROL WORD
DAOUT2	16	PVM ANALOG OUTPUT CHANNEL #2 AND #5 CONTROL WORD
DAOUT3	18	PVM ANALOG OUTPUT CHANNEL #3 AND #6 CONTROL WORD
DATTBL	20	DUAL PORT RAM ADDA DATA PACKET TABLE (120 WORDS)
DISCI1	22	DUAL PORT RAM ADDA DISCRETE INPUTS WORD 1
DISCI2	24	DUAL PORT RAM ADDA DISCRETE INPUTS WORD 2
DISCI3	26	DUAL PORT RAM ADDA DISCRETE INPUTS WORD 3
DISOUT	28	PVM DISCRETE LAMP/ADI OUTPUT FLAGS WORD
DMPTBL	30	DUAL PORT RAM ADDA DUMP TABLE (128 WORDS)
GSTCMD	32	PVM GUIDANCE SWITCHING UNIT START COMMAND I/O PORT
GFORCE	34	PVM BITE GUIDANCE MANIPULATOR FLAGS BYTE
PPINP1	36	DUAL PORT RAM ADDA PROGRAM PIN DATA WORD 1
PPINP2	38	DUAL PORT RAM ADDA PROGRAM PIN DATA WORD 2
PPROGD	40	DUAL PORT RAM ADDA PROGRAMMABLE DISCRETE CONFIGURATION WORD
PVMCOM	42	DUAL PORT RAM PVM TO ADDA COMMAND PORT (8 WORDS)
SCTBL	44	DUAL PORT RAM ADDA SCALING TABLE (1024 WORDS)
SERBUS	46	DUAL PORT RAM ADDA SERIAL BUS CONFIGURATION TABLE (4 WORDS)
TRN429	48	429 TRANSMIT PACKET (4 WORDS)
TRW1	50	PVM REQUESTED TEST ADDRESS WORD
VTVOL	52	PVM AUDIO VOLUME CONTROL SETTING BYTE
ADASUM	54	DUAL PORT RAM ADDA CHECKSUM OF CONFIGURATION DATA (2 WORDS)
GUICON	56	DUAL PORT RAM ADDA GUIDANCE CONSTANTS (27 WORDS)
CPUFL	58	PVM BITE RESULT FLAG BYTE, INCREMENTAL CPU TEST
RAMFL	60	PVM BITE RESULT FLAG BYTE, INCREMENTAL RAM TEST
ROMFL	62	PVM BITE RESULT FLAG BYTE, INCREMENTAL ROM TEST
WCHFL	64	PVM BITE RESULT FLAG BYTE, WATCHDOG TIMER TEST
WAITFL	66	PVM BITE RESULT FLAG BYTE, WAIT STATE HARDWARE TEST
ANATFL	68	PVM BITE RESULT FLAG BYTE, ANALOG HARDWARE TEST
WRMSFL	70	PVM BITE RESULT FLAG BYTE, WARM START TEST
VOITFL	72	PVM BITE RESULT FLAG BYTE, VOICE TEST
DMDCFL	74	PVM BITE RESULT FLAG BYTE, DATA MODULE CRC TEST
NVMFLG	76	PVM BITE RESULT FLAG BYTE, NON-VOLATILE MEMORY TEST
SYSTFL	78	PVM BITE RESULT FLAG BYTE, OPERATING SYSTEM TEST
DPRFAI	80	PVM BITE RESULT FLAG BYTE, DUAL PORT RAM TEST
WARMST	82	PVM WARM-START BOOLEAN BYTE
ADATST	84	DUAL PORT RAM PVM TO ADDA TEST REQUEST COMMAND WORD

PVM Indirect Address Table
Figure 116 (Sheet 1)

REGISTER	OFFSET	DESCRIPTION
CURMSG	86	PVM ADDRESS WORD OF THE NEXT MESSAGE TO BE ANNUNCIATED
CURFLT	88	PVM CURRENT INTERNAL SYSTEM FAULTS ARRAY WORDS
FAILCT	90	PVM FAILED STATES COUNTERS BYTE
ADATMO	92	ADDA WATCHDOG TIMER COUNTER WORD

PVM Indirect Address Table
Figure 116 (Sheet 2)

OFFSET	DEFINITION
0000H	10K Calibration Resistor
0001H	Power Supply Mod Resistor
0002H	ADDA Mod Resistor #1
0003H	ADDA Mod Resistor #2
0004H	PVM Mod Resistor #1
0005H	PVM Mod Resistor #2
0006H	First Officer Roll Command
0007H	First Officer Pitch Command
0008H	Captain Roll Command
0009H	Captain Pitch Command
000AH	First Officer GSU Status
000BH	Captain GSU Status
000CH	First Officer Fast/Slow Command
000DH	Captain Fast/Slow Command

ADCDAT Table Organization
Figure 117

NOTE: The parameter word(s) must be entered before the actual command word.

The ADDA system assumes a command is complete and ready for execution wherever the command word is non-zero. It acknowledges the command by zeroing the command word. Command errors are reported by the ADDA by setting the command word to FFFFH. This can occur if the command requests an illegal function such as attempting to read a RAM position not mapped to RAM. If this occurs, zero the command word to clear the condition.

The scratch pad is used by all commands that retrieve data from the ADDA. The scratch pad is located in dual ported RAM at address 8F00H and is referenced by the mnemonic DMPTBL. This address is within PVM address space and is viewed using the DW command (refer to paragraph D.).

It is not recommended to attempt commands not listed. Although other commands may exist, they may perform functions not supportive of the test effort and can cause the system to perform in unexpected ways. Care should be taken in constructing commands because errant commands may cause the system to perform erratically.

COMMAND	DEFINITION
0001H	Dump P1 (1 to 128) ADDA RAM words to the scratch pad, beginning at address P2.
0002H	Dump P1 (1 to 128) ADDA ROM words to the scratch pad, beginning at address P2.
0003H	Dump seven ADDA RAM words to the scratch pad. (P1 through P7 specify desired addresses.) (All parameters must be used.)
0006H	Set the ADDA RAM word at address P1 to value P2.
0007H	Oump byte input from ADDA I/O port P1 to scratch pad.
0008H	Dump word input from ADDA I/O port P1 to scratch pad.
0009H	Output byte value in P2 to ADDA I/O port P1.
000AH	Dutput word value in P2 to ADDA I/O port P1.
0013H	Set the ADDA RAM byte at address P1 to value P2.

ADDA Command Word Table
Figure 118

REGISTER	OFFSET	DESCRIPTION
CIB_SIZE	0 (0x0112)	Conversion information block size word
CIB_TABLE	2	Conversion information block table (word)
TRCVFLT	4	429 transcelver fault flags word
LATCHLOCK	6	Discrete output latch lock word

ADDA Indirect Address Table
Figure 119

K. ADDA Indirect Address Table

The ADDA software contains an indirect address table located in ROM at address 0112H. Variables like LATCHLOCK can be relocated because of software changes, so its address should be determined through the ADDA indirect address table (refer to Figure 119). The structure of the table is constant with additions appended to the end of the list. Each entry is a 16-bit word address pointer. When troubleshooting with the RS232 interface, use entries from this table.

The pointer table can be dumped using the following command sequence (address 801EH is used for PVMCOM and address 06E0H is used for the variable LATCHLOCK) (refer to Figure 119):

```
EXAMPLE:

>CW
Address? 8020
8020:  0000/0004     Set the length parameter P1
8D20:  0004
8022:  0000/0112     Set the requested address P2
8D22:  0112
```

```
8024:  0000/ U        Terminate current command
>

>CW
Address? 801E
801E:  0000/0002      Set command word to dump ADDA ROM
801E:  0002
8020:  0004/ U
>

>DW
Address? 8F00         Read requested data in dump table
How many? 0A          Use >8 to eliminate monitor mode
8F00:  000A0510 0400 06E0 FFFF FFFF FFFF FFFF
8F10:  FFFF FFFF
>
```

L. Special ADDA Debugging Mechanisms

The ADDA subsystem software contains a variable LATCHLOCK (located through the ADDA indirect address table) that possesses the ability to disable the ADDA low level driver use of the input signal mux LATSL2. This is done by writing the pattern 5A5AH into the variable LATCHLOCK. LATSL2 can then be directly programmed using the output word command (refer to the ADDA command word table) to switch any two-wire or three-wire signal onto the ADDA ADCs.

The following example assumes that the address of PVMCOM is 801EH and that the address of LATCHLOCK is 0506H (refer to the PVM and ADDA indirect address tables for actual addresses). Disable ADDA drivers from using LATSL2.

```
EXAMPLE:

>CW
Address? 8020
8020:  0000/0506      Set P1 to address LATCHLOCK
8020:  0506
8022:  0000/5A5A      Set P2 to disable pattern
8022:  5A5A
8024:  0000/ U        Terminate current CW command
>

>CW
Address? 801E
801E:  0000/0006      Set command word to set AODA RAM word
801E:  0006
8020:  0560/ U
>
```

Select the two-wire Mach input onto the ADDA ADCs by writing the value 0003H to LATSL1. Refer to DESCRIPTION AND OPERATION, Figure 28 for details on the LATSL1 settings.

```
EXAMPLE:

>CW
Address? 801E
```

```
801E:  0000/          Checking status of last command (0H ok)
801E:  0000
8020:  0560/5100      Set P1 to LATSL1
8020:  5100
8022:  5A5A/0003      Select Mach two-wire input
8022:  0003
8024:  0000/ U        Terminate command
>
```

14. **Troubleshooting Examples**

NOTE: *Refer to the GSE Hardware User's Guide, Document 951-6517-603; Software User's Manual, Document 998-1394-600; and Software Implementation Document, Document 998-1394-660, to prepare to use the MKVII WC GSE to troubleshoot a UUT. These documents are included with the MKVII WC GSE.*

A. Example 1, Failed 600-Ohm Audio Output

(1) Turn off the GSE system power.

(2) Open the MKVII door with the PVM board attached to it.

(3) Turn on the GSE power (both 115 VAC 60Hz and the 115 VAC 400Hz).

(4) Initialize the MKVII Terminal mode (refer to one of the following):

NOTE: *Initialization can be repeated at any time and should be performed when problems arise with the interface.*

(a) Hold the CTRL key down and press the Z key. After these keys are released, press the ENTER key.

(b) Select the INITIALIZE push button at the bottom of the terminal screen.

(5) A header and prompt (>) should be transmitted by the MKVII and displayed on the screen.

(6) Use the OB command to output any value to address 5181H. Writes to this address reset the voice chip.

(7) Use the OB command to output any value to address 5701H. Writes to this address enable the voice chip.

(8) Use the OB command to output FFH to address 50E1H. This programs the voice gain amplifier for maximum output (0H = mute, FFH = maximum).

(9) Use the OB command to output a value to address 5021H. This commands the voice chip to say a phrase. Valid values are found in DESCRIPTION AND OPERATION, Figure 42.

NOTE: *Only every other voice can be output through this mechanism.*

(10) Use an oscilloscope to probe back through the 600-ohm audio circuit and look for the point where the pulse should be (but is not).

NOTE: *If the circuit indicates no failure, but no output of the audio circuit is present, the problem may be a faulty flex cable.*

B. Example 2, Failed Two-Wire DC Radio Altitude Test

(1) With the UUT installed on the GSE, open the door of the UUT with the ADDA board attached. Make sure power is applied to the GSE.

(2) Use a DMM to measure the voltage at the input pins of AR3A (flex cables, J-11 pin-6 and pin-7). Remove the rubber protection strip from the flex cables.

(3) Use the following formula to calculate the gain of AR3A:

$[(0.243)\ (V_L - V_H)] + 4.39$ (offset voltage)

V_L = Voltage on flex cable J11-6
V_H = Voltage on flex cable J11-7

(4) Put the DMM leads on the input of the multiplexer (U2 pin-4).

(5) Determine the address of the LATCHLOCK variable from the ADDA indirect address table. (Refer to paragraph 13.E. for details on retrieving ROM data from the ADDA using the PVMCOM port.)

(6) Set the ADDA RAM variable LATCHLOCK to 5A5AH. This disables ADDA ability to switch the LATSL2 setting.

(7) Use the PVMCOM port to output 0003H to address 4200H on the ADDA. This sets LATSL2 for a DC gain factor of 1. (Refer to DESCRIPTION AND OPERATION, Figure 27 for a description of LATSL2.)

(8) Use the PVMCOM port to output 000H to address 5100H on the ADDA. This sets LATSL1 to switch radio altitude and radio altitude validity inputs onto the ADDA ADCs. (Refer to DESCRIPTION AND OPERATION, Figure 28 for a description of LATSL1.)

(9) If the input and output of the mux is the same value, that would indicate the mux is ok.

If the ATP listed multiple two-wire failures, the muxes and ADCs should be checked for failures.

If the gain select circuit has too much or too little gain, the ATP should have listed that as a failure.

If the output signal from the output of AR12 pin-6 is clipping, the input limiter circuit may be over-driving.

(10) Repeat steps (7) and (8) using channel 0EH to select the 2.5V ADC reference.

(11) Use the PVMCOM port to set the ADDA RAM word address 9000H. This initiates an ADC conversion.

Use the PVMCOM port to read ADDA RAM words at address 0A000 through 0A003. These are data and status registers for ADDA ADC #1.

Use the PVMCOM port to set the ADDA RAM words at address 0B000 through 0B003. These are the data and status registers for ADDA ADC #2.

Use an oscilloscope to look for a pulse on U21 pin-1.

(12) Use the following equations to determine if the output from the ADC is correct.

(a) $5/2^{14}$ resolution = value of least significant bit (LSB).

(b) Convert HEX value to binary, 2CCC = 0010 1100 1100 1100

(c) Shitt right bits 00 1011 0011 0011 (00), added by the ADC when the data is put on the 16-bit bus, are removed.

Check the sign bit. Sign bit set = positive, not set = negative. (00 0000 0000 0000 = -5V, 10 0000 0000 0000 = 0V, 11 1111 1111 1111 = +5V)

(d) Determine the binary value of 00 1011 0011 0011. 2048 + 512 + 256 + 32 + 16 + 2 + 1 = 2867.

(e) Multiply 2867 by 610 * 10^{-6} = 1.75.

(f) Subtract the +5V reference from 1.75 = -3.25V.

(13) The input to the ADC should be -3.25V. If it is not, proceed using standard troubleshooting techniques.

C. Example 3, PVM Analog Output Test Failure

For this example, it is important to understand the schematic, because the PVM does not identify what output relates to the GSE reporting. Identifying the failed output is simplified by noting a common point for the output of U18 for CAPPITCH and FOPITCH. This is true for the other two outputs from U18.

(1) Power up the UUT and initialize the MKVII Terminal mode (refer to one of the following):

NOTE: Initialization can be repeated at any time and should be performed when problems arise with the interface.

(a) Hold the CTRL key down and press the Z key. After these keys are released, press the ENTER key.

(b) Select the INITIALIZE push button at the bottom of the terminal screen.

(2) A header and prompt (>) should be transmitted by the MKVII and displayed on the screen.

(3) Locate the address for DAOUT1, DAOUT2, DAOUT3, and DACPAR variables from the PVM indirect address table.

(4) Use the CW command to set DACPAR, DACPAR+2, and DACPAR+4 to F000H. This sets the flight director output gain factors.

(5) Use the CW command to set DAOUT1, DAOUT2, and DAOUT3 to F000H. This sets the analog output voltages.

(6) Check for analog outputs of -2.5V on both the captain and first officer pitch command.

NOTE: If the captain recovery guidance signals are bad, and the first officer guidance signals are good, check the operation of the operational amplifier associated with the captain recovery guidance.

D. Example 4, PVM Analog #2 and #5 Test Fail

(1) Set up the GSE to run the Diagnostic software.

(2) Build a Diagnostic profile selecting the PVM ANALOG OUTPUT task and selecting the ANALOG OUTPUTS #2 and #5 ON/OFF tests. Run the profile.

(3) If the analog #5 test failed but the #2 test passed, turn off the power to the UUT, open the PVM door, and measure the resistance of R10.

(4) If the value of R10 is more than 100K ohms, R10 may be open.

(5) Measure the resistance of R9 or R7 if the R10 measurement is questionable.

(6) If R9 or R7 have the same resistance, check the output of the operational amplifier AR2B.

(7) If the resistor and operational amplifier resistance checks are good, check the operation of DAC U18 as follows:

Prepare to use an oscilloscope with the following settings:

```
DC Coupling
1-Channel
200 microseconds sweep speed
2V/division threshold
Auto trigger
```

(8) Customize the test execution as follows:

(a) From the Diagnostics main menu, select DIAGNOSTICS.

(b) When the Diagnostics menu opens, select CUSTOMIZE TESTS.

(c) Select the PVM ANALOG OUTPUT task.

(d) Customize Output #2 and #5 tests #1 and #2 by selecting test pause options:

```
√ Ready to Start the Test
√ UUT Output is Active
```

(9) Loop on the PVM analog output test profile until the problem is found (select 50 loops).

(10) Use the oscilloscope to observe pin-28 on U18. Use the oscilloscope probe to detect where the pulse is lost. Look for an open or short in the circuit and replace the faulty component. When the failed component is identified, press the F9 key to abort the Diagnostics profile.

E. Example 5, Power Supply Failure

If the power indicators on the front panel of the GSE dim, two possible problems can be the cause. The 115 VAC or 400Hz power may be faulty; or the power supply is receiving a reset signal from either the current limit circuit, over-voltage circuit, or under-voltage circuit. For this example, a problem with the UUT is discussed.

(1) Build a Diagnostic profile selecting the POWER SUPPLY task and selecting the +5V A/D REFERENCE test (customize the test control as needed).

(2) Loop the power supply test profile until the problem is found (50 loops).

(3) Use a DMM to measure the voltage on the cathode of D5. If the measurement is 5V, the +5VDC circuit is ok.

(4) Measure the voltage at the Q1 and Q2 base-emitter junction. If the reading is different by 0.6V, the ±12VDC is over-currenting.

(5) If the problem continues, disconnect the flex cables between the ADDA, PVM, and the power supply one by one. Watch to see if the 400Hz lamp on the GSE front panel stays on with full brightness.

(6) If the problem with the power supply is with the over-voltage monitor circuits, check the voltage of D3, D4, D5, and D6 cathodes. If any of them are low, the problem is likely to be found in that circuit.

(7) When the failed component is identified, press the F9 key to abort the Diagnostics profile.

F. Example 6, Voice Annunciation Failure

NOTE: *All address values are in normal I/O space. Message number values must be written in word mode.*

(1) Power up the UUT and initialize the MKVII Terminal mode (refer to one of the following):

NOTE: *Initialization can be repeated at any time and should be performed when problems arise with the interface.*

(a) Hold the CTRL key down and press the Z key. After these keys are released, press the ENTER key.

(b) Select the INITIALIZE push button at the bottom of the terminal screen.

(2) A header and prompt (>) should be transmitted by the MKVII and displayed on the screen.

(3) Use the OB command to output any value to address 5181H. Writes to this address reset the voice chip.

(4) Use the OB command to output any value to address 5701H. Writes to this address enable the voice chip.

(5) Use the OB command to output FFH to address 50E1H. This programs the voice gain amplifier for maximum output (0H = mute, FFH = maximum).

(6) Use the OB command to output a value to address 5021H. This commands the voice chip to say a phrase. Valid values are found in DESCRIPTION AND OPERATION, Figure 42.

NOTE: *Only every other voice can be output through this mechanism.*

G. Example 7, Voice Circuit Using Test Pulse

The following steps (1) through (11) describe how to use a test pulse to troubleshoot a failed circuit.

(1) Power up the UUT and initialize the MKVII Terminal mode (refer to one of the following):

NOTE: *Initialization can be repeated at any time and should be performed when problems arise with the interface.*

(a) Hold the CTRL key down and press the Z key. After these keys are released, press the ENTER key.

(b) Select the INITIALIZE push button at the bottom of the terminal screen.

(2) A header and prompt (>) should be transmitted by the MKVII and displayed on the screen.

(3) Use the OB command to output 07H to address 50E1H. This programs the voice gain amplifier (0H = mute, FFH = maximum).

(4) Use the OB command to output any value to address 5181H. Writes to this address reset the voice chip.

(5) Use the OB command to output any value to address 5701H. Writes to this address enable the voice chip.

(6) Use the OB command to output a value to address 5021H. This commands the voice chip to say a phrase. Valid values are found in DESCRIPTION AND OPERATION, Figure 42.

NOTE: *Only every other voice can be output through this mechanism.*

(7) Use the IB command to input a byte from the address 5081H. This reads the miscellaneous

input port.

(8) Make sure bits #6 and #7 are low. (Bit #6 = 600 ohms, bit #7 = 8 ohms.)

(9) Use the OB command to output 3DH to address 5021H. This will command the voice chip to issue a test pulse.

(10) Use the IB command to input a byte from the address 5081H. This reads the miscellaneous input port.

(11) Make sure bits #6 and #7 are low. (Bit #6 = 600 ohms, bit #7 = 8 ohms.)

NOTE: A soft click sound may be audible when this test is executed.

H. Example 8, ADC (Address 5041H, Normal I/O Space, Read/Write)

NOTE: Refer to paragraph 15.N. for mux channels.

(1) Power up the UUT and initialize the MKVII Terminal mode (refer to one of the following):

NOTE: Initialization can be repeated at any time and should be performed when problems arise with the interface.

(a) Hold the CTRL key down and press the Z key. After these keys are released, press the ENTER key.

(b) Select the INITIALIZE push button at the bottom of the terminal screen.

(2) A header and prompt (>) should be transmitted by the MKVII and displayed on the screen.

(3) Generate an analog output as specified in Example 3.

(4) Use the DW command to display memory at location ADCDAT. (Refer to the PVM indirect address table in Figure 116 and ADC read back in paragraph 13.H.)

(5) Make sure the read back displays a value of approximately 00C0H.

(6) Re-execute Example 3 using FFFH for the DAOUT1 value. This will generate a -2.5V DC output value resulting in an approximate read back value of 0044H.

15. **Memory Maps and Decoding Memory Devices**

In order to be able to test and interpret results, the following pages include memory maps and PAL equations.

A. **ADDA Memory Map**

PIN #	NAME	INPUT/OUTPUT
2	CLK1 (8Mhz)	INPUT
3	ZPCS4	INPUT
4	ZMCS3	INPUT
5	ZMCS2	INPUT
6	ARDY	OUTPUT
7	2WM1EN	OUTPUT
8	2WM2EN	OUTPUT
9	2WM3EN	OUTPUT
10	2A3	INPUT
11	2A4	INPUT
12	LATSL2	OUTPUT
13	Z429WR	OUTPUT
16	ADRST	OUTPUT
18	ZMCS1	INPUT
19	XZRST	INPUT
20	ZRES	INPUT
21	Z429CS	INPUT
24	CLK2 (8Mhz)	INPUT
25	A0	INPUT
26	BHE	INPUT
27	ZWR	INPUT
28	ZBUSYL (from PVM)	INPUT
37	4Mhz	OUTPUT
38	ZLCSHI	OUTPUT
40	ZLCSLO	OUTPUT
42	LCS	INPUT
43	RESET	INPUT (not used)

NOTE: Pins 14, 15, 29-36 are not connected.

B. Output Equations

```
- ARDY   = /ZBUSYL + /MCS1 - ADRST = /XZRST + 2A3 * 2A4 * (/MCS2 * /MCS3)
- 2WM1EN = /2A3 * /2A4 - 4MHz = 4MHz
- 2WM2EN = 2A3 * /2A4 - ZLCSHI = /LCS * /A0
- 2WM3EN = /2A3 * 2A4 - ZLCSLO = /LCS * /BHE
- LATSL2 = /PCS4 * /ZWR
- Z429WR = /ZWR
```

C. ADDA Gate Array (U53)

The gate array contains a Watchdog timer, interrupt controller, chip selects, RS232 controller and UART (not used).

INPUTS: PIN #	NAME	PIN #	NAME
4	ZWR	7	ZRD
8	XZRST	11	ZLOCK
16	ZINTA	17	REFINT
18	EOC1	20	ZAD1CS
21	ZAD2CS	23	LHIT0
24	LHIT1	25	LHIT2
26	RXD (not used)	27	DOGENA
28	PVMZADDA (gnd=ADDA)	29	CPUCLK
33	A0 (A1)	34	A5
35	A6	36	A7
37	A8	38	A9
39	A10	40	A11
41	A12	42	A13
43	A14	44	A15
78	S2	81	ALE
OUTPUTS:			
46	DOGSTAT	47	TXD (not used)
48	GINT	53	CLK244HZ
62	ZINT3	65	ZPPIN2
67	ZPPIN0	68	ZACTWR
71	LATSL1	76	ZADRD
77	ZRES		
COMBINATION I/O:			
1	D3	5	D4
6	D5	9	D6
10	D7	79	D0
80	D1	84	D2
POWER:			
VDD (+5Vdc) pins 3, 31, 51, 72			
VSS (Ground) pins 13, 45, 58, 82			

NOTE: *All pins not listed are not used and should be tied to the VDD or VSS as listed on the ADDA schematic.*

D. ADDA Gate Array Equations

```
- DOGSTAT  = A(5021 - 503F) * /S2 */ZWR * /ALE * A0(G.A.) + /XZRST
- TXD is RS232 output, not used, software removed
- CLK244HZ = 200 Hz Clock out
- ZINT3    = goes LOW for 2 clock pulses (clock at 4Mhz) at receipt of REFINT
- ZPPIN2   = /(A(51C0 - 51DE) * /S2 * /ZRD * /ALE * /A0(G.A.)
- ZPPIN0   = /(A(5180 - 51BE) * /S2 * /ZRD * /ALE * /A0(G.A.)
- ZACTWR   = /(A(5141 - 517F) * /S2 * /ZRD * /ALE * /A0(G.A.)
- ZADRD    = /(/ZAD1CS + /ZAD2CS) * /ZRD)
- ZRES     = (/WCHDOG (internal G.A.) + /DOGENA) * XZRST
- LATSL1   = A(5100 - 513E) * /S2 * /ZWR * /ALE * /A0(G.A.)
```

NOTE: *(G.A.) means input A0 on Gate Array. Actual address line is A1.*

NOTE: *RXD (RS232 RCV) is not used, software removed. Pin 27 (DOGENA), when grounded, will disable watchdog timer. Pin 28 (PVMZADDA) determines Gate Array operation; +5Vdc = PVM, GND = ADDA.*

E. PVM Memory Map

CODE SPACE

ADDRESS	(EVEN ADDRESSES)	(ODD ADDRESSES)	ADDRESS
0000			0001
	PROGRAM MODULE (87257)	PROGRAM MDDULE (87257)	READ ONLY
FFFE			FFFF
D 15 D 14 D 13 D 12 D 11 D 10 D 9 D 8		D 7 D 6 D 5 D 4 D 3 D 2 D 1 D 0	

DATA SPACE

ADDRESS	(EVEN ADDRESSES)	(ODD ADDRESSES)	ADDRESS
0000	PROGRAM MOOULE	PROGRAM MOOULE	0001 READ ONLY
7FFE	(FUTURE EXPANSION)	(FUTURE EXPANSION)	7FFF
8000	DUAL PORT RAM 6142 (SLAVE)	DUAL PORT RAM 6132 (MASTER)	8001 READ/WRITE 8FFF
9000	RAM (FUTURE EXPANSION)	RAM (FUTURE EXPANSION)	9001 READ/WRITE
BFFE	(20256)	(20256)	BFFF
C000	RAM (6164)	RAM (6164)	C001 READ/WRITE
FFFE			FFFF
D 15 D 14 D 13 D 12 D 11 D 10 D 9 D 8		D 7 D 6 D 5 D 4 D 3 D 2 D 1 D 0	

SPECIAL I/O SPACE

ADDRESS	(EVEN ADDRESSES)	(ODD ADDRESSES)	ADDRESS
0000			0001
	PROGRAM MODULE (87257) (READ ONLY)	PROGRAM MODULE (87257) (READ ONLY)	
FFFE			FFFF
D 15 D 14 D 13 D 12 D 11 D 10 D 9 D 8		D 7 D 6 D 5 D 4 D 3 D 2 D 1 D 0	

NORMAL I/O SPACE

(EVEN ADDRESSES)	(ODD ADDRESSES)	ADDRESS	R/W	WAIT STATES
		0001		
RESERVED FOR DUAL PORT RAM			R,W	0
		0FFF		
XXXXXXXXXXXXXXXXXXX		1001		
XXXXXXXXXXXXXXXXXXX	EEPROM (28C64)		R,W	0
XXXXXXXXXXXXXXXXXXX	(READ/WRITE)	4FFF		
XXXXXXXXXXXXXXXXXXX	ZDISCO; LAMP DR. LATCH	5001	W	0
XXXXXXXXXXXXXXXXXXX	ZVOICE; OUTPUT MSG.	5021	W	1
XXXXXXXXXXXXXXXXXXX	ZRIDAD; RIDENT A/D EN.	5041	R,W	2
XXXXXXXXXXXXXXXXXXX	UART DATA REGISTER	5061	R,W	0
XXXXXXXXXXXXXXXXXXX	ZMISCI; MISC. INPUTS	5081	R	0
XXXXXXXXXXXXXXXXXXX	MUXALE; RIDENT MUX	50C1	W	0
XXXXXXXXXXXXXXXXXXX	ZLOUDDA; LOUDNESS D/A	50E1	W	0
XXXXXXXXXXXXXXXXXXX	ZCLKDOG; RESTART WDOG	5101	W	0
XXXXXXXXXXXXXXXXXXX	IMREG; INT MASK REG	5141	R,W	0
XXXXXXXXXXXXXXXXXXX	INTSTAT; INT STAT REG	5161	R	0
XXXXXXXXXXXXXXXXXXX	ZVOIRST; RST VOICE CHIP	5181	W,DS	0
ZGUIDAT (GUIDANCE DAC)		5200-52FF	R,W	2
XXXXXXXXXXXXXXXXXXX	ZGUIDCTL (GUID SELECT)	5301	W,DS	0
XXXXXXXXXXXXXXXXXXX	ZGUIDMON (GUIDE DOG)	5401	W,DS	0
XXXXXXXXXXXXXXXXXXX	ZWARMTEST	5501	W	3
XXXXXXXXXXXXXXXXXXX	OK TO READ FOR WAIT ST.			
XXXXXXXXXXXXXXXXXXX	VOICE ENABLE	5701	W,DS	0
		5801		
	UNUSED		U	
		7FFX		
		8000		
DATA MODULE (8K X 16)			R	0
		FFFF		

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8		D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

NOTE: R = READ, W = WRITE, DS = QUALIFIED WITH ZDS, U = UNDEFINED.

F. DECODER EQUATIONS

INTERMEDIATE EQUATIONS:

```
CDDS = ST3 * ST2 * /ST1
DATS = ST3 * /ST2 * /ST1
SIO  = /ST3 * /ST2 * ST1 * ST0
NIO  = /ST3 * /ST2 * ST1 * /ST0
HBEN = /BZW * /A0
LBEN = /BZW * A0
VIACK = /ST3 * ST2 * ST1 * ST0 * /ZDS
NVIACK = /ST3 * ST2 * ST1 * /ST0 * /ZDS
```

```
      CONTROL SIGNAL EQUATIONS:

ZNVI   = /(NVIACK + /ZRESET); Reset equation for TIMINT latch
                  ; Set occurs every 4.096 msec automatically
ZRESET = / ((/XZRST + WDOGTO + ZMMODIN + ZIDMIN)
         * (/XZRST + ZRSTDISABLE))
DOGSTAT = (LATCH WDOGTO * (XZRST + /ZRSTDISABLE)); 1=WDOG, 0=XZRST
ZMODPWR = /(/ZIDMIN * /ZMMODIN)
ZRD     = /(RZW * /ZDS)
ZWR     = /( /RZW * /ZDS)
ZDBUSEN = /(( /ZDS + /RZW) * (ZPGMOD * ZDATMOD) * /BUSFLOAT)
ZWAIT:  ONE WAIT STATE = ZVOICE, ZDPRAMBSY
        TWO WAIT STATES = ZRIDAD, ZGUIDAT
        THREE WAIT STATES = ZWARMTEST
ZCLKDOG = /(/ZWR * (ADRS = 5101H))

     MEMORY DEVICE CHIP SELECTS:

ZPGMOD  = /(( CODS + (DATS * /A15)) * RZW + SIO)
ZDATMOD = /(A15 * NIO * RZW)
MAD16   = DATS
ZRAMHB  = /(A15 * (A14 + A13 + A12) * DATS * HBEN);9000-FFFF,DATA SPACE
ZRAMLB  = /(A15 * (A14 + A13 + A12) * OATS * LBEN);9000-FFFF,DATA SPACE
ZEEPCS  = /((((/A15 * /A14 * /A13 * A12)
          + (/A15 * /A14 * A13 * /A12)
          + (/A15 * /A14 * A13 * A12)
          + (/A15 * A14 * /A13 * /A12)) * AO * NIO)
ZDPRAM  = /(A15 * /A14 * /A13 * /A12 * DATS)
          ;8000-8FFF, DATA SPACE, WORD MODE ONLY

        I/O DEVICE CHIP SELECTS:

DISCOLAT  = (A5001 - 501F * /RZW * NIO * AO * ZDS)
ZWARMTEST = /(A5501 - 56FF * NIO * AO)
ZRIDAD    = /(A5041 - 505F * NIO * AO)
ZMUXALE   = (/ZWR * (ADRS = 50C1H)); DATA = MUX CHAN #
ZGUIDAT   = /(A5200 - 52FF * NIO); GUIDANCE DAC
ZGUIDCTL  = /(A5301 - 53FF * /RZW * NIO * AO * /ZDS); GUID. SELECT
ZGUIDMON  = /(A5401 - 54FF * /RZW * NIO * AO * /ZDS); GUID. WATCHDOG

        VOICE SUB-SYSTEM SIGNALS:

ZVOICE   = /(A5021 - 503F * /RZW * NIO * AO)
ZVOICPR1 = /((LATCH /ZVOICE * /ZDS * /D8) * /ZDRQ); MSG# 0 - 255
ZVOICPR2 = /((LATCH /ZVOICE * /ZDS * /D8) * /ZDRO); MSG# 256 - 511

ZVOIRST:
RESET VOICE  = ((A5181 - 519F * /ZDS * /RZW * NIO * AO) + /ZRESET)
ENABLE VOICE = (A5701 - 57FF * /ZDS * /RZW * NID * AO)

ZLOUDDA = /(/ZWR * (ADRS = 50E1H)); DATA = AUDIO VOLUME
```

G. **UART Signals**

TXD = Serialize data written to address= 5061H

RXD: Serial data is converted to byte wide data and can be read from address 5061H. An interrupt is generated when new received data is available.

H. **Interrupt Controller Signals**

```
ZGINT = / (( RXRDY * IM0) + (TXEMPTY * IM1) + (INT2 * IM2)
        + (INT3 * IM3) + (INT4 * IM4) + (INT5 * IM5))

    Where:  IMx = Interrupt mask register bit X

INT_VECTOR     = D7..D0 * VIACK * /ZRD
INT_MASK_REG. = D7..D0 * (ADRS = 5141H) * (/ZRD + /ZWR)
INT_STAT_REG. = D7..D0 * (ADRS = 5161H) * /ZRD
```

I. **RAM Memory**

```
Size:  8K byte each (8K words total, expandable to 16K words)
Address:  9000 - FFFFH, data space
Data width:  16 bits
Wait states:  Zero
```

J. **Nonvolatile Memory**

Size: 8K bytes Address: 1001 - 4FFFH, odd only, normal I/O space Endurance: 100,000 cycles/byte

Data retention: 10 years Wait states: One added automatically for I/O transactions Write cycle time: 1 millisecond

The +5KA power supply is held up for at least 2 seconds; this allows a write cycle initiated prior to a system power failure to complete.

K. **Dual Port RAM**

```
IOT 7142 Slave DPRAM
Size:  2K X 8 each
Address:  8000 - 8FFFH, data space
0000 - 0FFFH, I/O space (unused)

Data width:  16 bits
Wait states:  Zero in data space
One I/O space
```

The master and slave RAM devices are identical, except that the bus arbitration scheme is controlled by the master device.

L. Miscellaneous Input Buffer (address 5081H, NIO space, Read only)

```
D0 = RSTSTS       (0 = PWR SUPPLY          1 = WDOG TIMEOUT)
D1 = ADIFLAG1     (0 = IN VIEW             1 = OUT OF VIEW)
D2 = ADIFLAG2     (0 = IN VIEW             1 = OUT OF VIEW)
D3 = GUIVAL       (0 = GUIDANCE FAULT      1 = VALID)
D4 = SWUMON       (0 = 28V BUS FAULT       1 = OK)
D5 = WARMSTART    (0 = COLD START          1 = WARM START)
D6 = Z600VAL      (0 = OK                  1 = 600-OHM AUDIO FAIL)
D7 = Z8VAL        (0 = OK                  1 = 8-OHM AUDIO FAILURE)
```

M. Discrete Outputs (Address = 5001H, NIO Space, Write Only)

BIT	NOMENCLATURE	REAR CONN	STATE	
D0 =	GLIDESLOPE ALERT LAMP	(J1A-21)	0 = OFF	1 = ON
D1 =	GLIDESLOPE CANCEL LAMP	(J1B-33)	0 = OFF	1 = ON
D2 =	GROUND PROX. WARNING LAMP	(J1B-11) (J1B-9) (J1A-13)	0 = OFF	1 = ON
D3 =	GPWC INOP. LAMP	(J1B-12)	0 = ON	*1 = OFF
D4 =	AUTO. BACKCOURSE ANNUNC.	(J1B-10)	0 = OFF	1 = ON
D5 =	WS PRE-ALERT LAMP	(J2-1A)	0 = OFF	1 = ON
D6 =	WINDSHEAR WARNING LAMP	(J2-2A)	0 = OFF	1 = ON
D7 =	WS SYS. FAILURE LAMP	(J2-3A)	0 = ON	*1 = OFF
D8 =	SPD. CMD. TAKEOFF MODE	(J2-15B)	0 = OFF	1 = ON
D9 =	GUIDANCE GSU DE-SELECT #2	(J2-14B)	0 = OFF	1 = DESEL.
D10 =	SPD. CMD. GO-AROUND MODE	(J2-13B)	0 = OFF	1 = ON
D11 =	GUIDANCE GSU SELECT #2	(J2-12B)	0 = OFF	1 = SELECT
D12 =	FLT. DIRECTOR OFF SELECT	(J2-11B)	0 = OFF	1 = SELECT
D13 =	GUIDANCE GSU DE-SELECT #1	(J2-7B)	0 = OFF	1 = DESEL.
D14 =	CAPTAIN'S ADI FLAG	(J2-11A)	0 = IN VIEW	1 = UNSEEN
D15 =	FIRST OFFICER'S ADI FLAG	(J2-5B)	0 = IN VIEW	1 = UNSEEN

The state of the lamps are latched. The latches are reset to 0 under any of the following conditions.

N. Mux Channels (Address = 50C1H, NIO Space, Write Only)

To select the mux channel, write data to address 50C1H per the following list.

DATA	INPUT CHANNEL
00	10.0K CALIBRATION RESISTOR
01	P/S MOD. RESISTOR (RPOWER)
02	ADDA MOD RES. #1 (RADDA1)
03	ADDA MOD RES. #2 (RADDA2)
04	PVM MOD RES. #2 (RPVM2)
05	PVM MOD RES. #1 (RPVM1)
06	F/O ROLL CMD. READBACK
07	WARMSTARTB SELF-TEST STATUS
0E	F/O PITCH CMD. READBACK
16	CAPT. ROLL CMD. READBACK
1E	CAPT. PITCH CMD. READBACK
26	FIRST OFFICERS GSU VALIDITY
2E	CAPTAINS GSU VALIDITY
36	F/O FAST/SLOW READBACK
3E	CAPT. FAST/SLOW READBACK

REVISION CODE	REVISION DESCRIPTION	SERIAL NO. EFFECTIVITY
1	Removed R221E from the spares listing and added it to U53 pin 16 (sheets 10 and 12).	All
	Changed notes to reflect actual note numbers on schematics (sheet 12).	All